

SAMSUNG

GSM TELEPHONE

SGH-E330

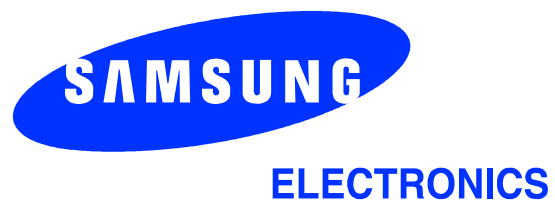
SERVICE *Manual*

GSM TELEPHONE



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1. SGH-E330 Specification

1. GSM General Specification

	GSM900 Phase 1	EGSM 900 Phase 2	DCS1800 Phase 1
Freq. Band[MHz] Uplink/Downlink	890~915 935~960	880~915 925~960	1710~1785 1805~1880
ARFCN range	1~124	0~124 & 975~1023	512~885
Tx/Rx spacing	45MHz	45MHz	95MHz
Mod. Bit rate / Bit Period	270.833kbps 3.692us	270.833kbps 3.692us	270.833kbps 3.692us
Time Slot Period / Frame Period	576.9us 4.615ms	576.9us 4.615ms	576.9us 4.615ms
Modulation	0.3GMSK	0.3GMSK	0.3GMSK
MS Power	33dBm~5dBm	33dBm~5dBm	30dBm~0dBm
Power Class	5pcl ~ 19pcl	5pcl ~ 19pcl	0pcl ~ 15pcl
Sensitivity	-102dBm	-102dBm	-100dBm
TDMA Mux	8	8	8
Cell Radius	35Km	35Km	2Km

2. GSM TX power class

TX Power control level	GSM900
5	33 ±3 dBm
6	31 ±3 dBm
7	29 ±3 dBm
8	27 ±3 dBm
9	25 ±3 dBm
10	23 ±3 dBm
11	21 ±3 dBm
12	19 ±3 dBm
13	17 ±3 dBm
14	15 ±3 dBm
15	13 ±3 dBm
16	11 ±5 dBm
17	9 ±5 dBm
18	7 ±5 dBm
19	5 ±5 dBm

TX Power control level	DCS1800
0	30 ±3 dBm
1	28 ±3 dBm
2	26 ±3 dBm
3	24 ±3 dBm
4	22 ±3 dBm
5	20 ±3 dBm
6	18 ±3 dBm
7	16 ±3 dBm
8	14 ±3 dBm
9	12 ±4 dBm
10	10 ±4 dBm
11	8 ±4dBm
12	6 ±4 dBm
13	4 ±4 dBm
14	2 ±5 dBm
15	0 ±5 dBm

2. SGH-E330 Circuit Description

1. SGH-E330 RF Circuit Description

1) RX PART

1. ASM(U103) Switching Tx, Rx path for GSM900, DCS1800 by logic controlling.

2. ASM Control Logic (U103) Truth Table

	VC1	VC2
GSM Tx Mode	H	L
DCS Tx Mode	L	H
GSM Rx Mode	L	L
DCS Rx Mode	L	L

3. FILTER

To convert Electromagnetic Field Wave to Acoustic Wave and then pass the specific frequency band.

- GSM FILTER (F100) For filtering the frequency band between 925 and 960 MHz
- DCS FILTER (F101) For filtering the frequency band between 1805 and 1880 MHz.

4. VC-TCXO (OSC100)

This module generates the 26MHz reference clock to drive the logic and RF. After additional process, the reference clock applies to the U100 Rx IQ demodulator and Tx IQ modulator. And then, the oscillator is controlled by serial data to select channel and use fast lock mode for GPRS high class operation.

5. Transceiver (U100)

The receiver front-end which amplifies the GSM, DCS aerial signal, converts the chosen channel down to a low IF signal of 100 kHz. The first stages are symmetrical low noise amplifiers (LNAs). They are matched to 50 ohm. The LNAs are followed by an IQ down mixer. It consists of two mixers in parallel but driven by quadrature out of phase LO signals. The In phase (I) and Quadrature phase (Q) IF signals are low pass filtered to provide protection from high frequency offset interferes. The low IF I and Q signals are then fed into the channel filter. The front-end low IF I and Q outputs enter the integrated bandpass channel filter with provision for five 8 dB gain steps in front of the filter.

2) TX PART

Baseband IQ signal fed into offset PLL, this function is included inside of U100 chip. OSC101 chip generates modulator signal which power level is about 6.5dBm and fed into Power Amplifier(U102). The PA output power and power ramping are well controlled by Auto Power Control circuit. We use offset PLL below table.

Modulation Spectrum	200kHz offset	GSM	-35dBc
	30 kHz bandwidth	DCS	-35dBc
	400kHz offset	GSM	-66dBc
	30 kHz bandwidth	DCS	-65dBc
	600kHz ~ 1.8MHz offset	GSM	-75dBc
	30 kHz bandwidth	DCS	-68dBc

2. Baseband Circuit description of SGH-E330

1. PCF50601

1.1. Power Management

Ten low-dropout regulators designed specifically for GSM applications power the terminal and help ensure optimal system performance and long battery life. A programmable boost converter provides support for 1.8V, 3.0V, and 5.0V SIMs, while a self-resetting, electronically fused switch supplies power to external accessories. Ancillary support functions, such as RTC module and High Voltage Charge pump, Clock generator, aid in reducing both board area and system complexity. I2C BUS serial interface provides access to control and configuration registers. This interface gives a microprocessor full control of the PCF50601 and enables system designers to maximize both standby and talk times.

Supervisory functions, including a reset generator, an input voltage monitor, and a temperature sensor, support reliable system design. These functions work together to ensure proper system behavior during start-up or in the event of a fault condition (low microprocessor voltage, insufficient battery energy, or excessive die temperature).

1.2. Backlight Brightness Modulator

The Backlight Brightness Modulator (BBM) contains a programmable Pulse-width modulator (PWM) and FET to modulate the intensity of a series of LED's or to control a DC/DC converter that drives LCD backlight.

But, this phone (SGH-E330) is use UFB LCD. UFB LCD controls backlight brightness by contrast setting.

So "BL_VDD" voltage is always high value when phone is in active mode. When phone is in dimming mode "BL_VDD" goes to about 10% duty PWM.

1.3. Clock Generator

The Clock Generator (CG) generates all clocks for internal and external usage. The 32768 Hz crystal oscillator provides an accurate low clock frequency for the PCF50601 and other circuitry.

2. LCD Connector

LCD is consisted of main LCD(color 65K UFB LCD) and sub LCD(color 65K UFB LCD).

Chip select signals LCD_MAIN_CS and LCD_SUB_CS, can enable Each LCD. BACKLIGHT signal enables white LED of main LCD. "RESET_2V8" signal initiates the reset process of the LCD.

16-bit data lines(LD(0)~LD(15)) transfers data and commands to LCD through bypass capacitor. Data and commands use "RS" signal. If this signal is high, inputs to LCD are commands. If it is low, inputs to LCD are data.

The signal which informs the state of LCD is whether input or output, is required. But in this system, there is no input state from LCD. So only "L_WR" signal is used to indicate write data or command to LCD. Power signals for LCD are "VBAT and "VDD2".

"M_SCL", "M_SCA", "PCLK", "FVALID", "LVALID" and "STANDBY" signals are all related to camera working.

"CAMERA_FLASH_SUPPLY" is voltage supply to flash led , and "SVC_LED" is signal for service led when the signal is low led is on and vice versa. "SPK_P" and "SPK_N" are used for audio speaker containing voice or melody. And

"VDD_VIB" from PCF50601 enables the motor.

3. Key

This is consisted of key interface pins among OM6359, KBIO(0:7). These signals compose the matrix. Result of matrix informs the key status to key interface in the OM6359. Power on/off key is separated from the matrix. So power on/off

signal is connected with PCF50601 to enable PCF50601. Fifteen key LEDs are use the "VBAT" as supply voltage. "VDD_KEY" signal enables LEDs. "FLIP" informs the status of folder (open or closed) to the OM6359. This uses the hall effect IC, SH248CSP. A magnet under main LCD enables SH248CSP.

4. EMI ESD Filter

This system uses the EMI ESD filter, EMIF09 to protect noise from IF CONNECTOR part.

5. IF connetor

It is 18-pin connector. They are designed to use VBAT, V_EXT_CHARGE, TXD0, RXD0, RTS0, CTS0, JIG_REC, CHARGER_OK, RXD1, TXD1, AUX_MIC, AUX_SPK and GND. They connected to power supply IC, microprocessor and signal processor IC.

6. Battery Charge Management

A complete constant-current/constant-voltage linear charger is used for single cell lithium-ion batteries. If TA connected to phone, "V_EXT_CHARGE" enable charger IC and supply current to battery. When fault condition caused, "CHG_ON" signal level change low to high and charger IC stop charging process.

7. Audio

EARP_P and EARP_N from OM6359 are connected to the main speaker. AUXSP is connected to the Hands free kit. MIC_P and MIC_N are connected to the main MIC. And AUX_MIC_P and AUX_MIC_N are connected to the Hands free kit.

YMU762C is a LSI for portable telephone that is capable of playing high quality music by utilizing FM synthesizer and ADPCM decoder that are included in this device.

As a synthesis, YMU762C is equipped 32 voices with different tones. Since the device is capable of simultaneously generating up to synchronous with the play of the FM synthesizer, various sampled voices can be used as sound effects. Since the play data of YMU762C are interpreted at anytime through FIFO, the length of the data(playing period) is not limited, so the device can flexibly support application such as incoming call melody music distribution service. The hardware sequencer built in this device allows playing of the complex music without giving excessive load to the CPU of the portable telephones. Moreover, the registers of the FM synthesizer can be operated directly for real time sound generation, allowing, for example, utilization of various sound effects when using the game software installed in the portable telephone.

YMU762C includes a speaker amplifier with high ripple removal rate whose maximum output is 550mW (SPVDD=3.6V). The device is also equipped with conventional function including a vibrator and a circuit for controlling LEDs synchronous with music.

For the headphone, it is provided with a stereophonic output terminal.

For the purpose of enabling YMU762C to demonstrate its full capabilities, Yamaha purpose to use "SMAF:Synthetic music Mobile Application Format" as a data distribution format that is compatible with multimedia. Since the SMAF takes a structure that sets importance on the synchronization between sound and images, various contents can be written into it including incoming call melody with words that can be used for training karaoke, and commercial channel that combines texts, images and sounds, and others. The hardware sequencer of YMU762C directly interprets and plays blocks relevant to synthesis (playing music and reproducing ADPCM with FM synthesizer) that are included in data distributed in SMAF.

8. Memory

Signals in the OM6359 enable two memories. They use only one volt supply voltage, VDD3 in the PCF50601. This system uses Samsung's memory, KBB06A500M-T402. It is consisted of 128M bits flash NOR memory and 128M bits flash NAND memory and 64M bits SCRAM. It has 16 bit data line, HD[0~15] which is connected to OM6359 and MV317S. It has 26 bit address lines, HA[1~26]. CS_NAND and NCSRAM signals are chip select. Writing process, HWR_N is low and it enables writing process to flash memory and SRAM. During reading process, HRD_N is low and it enables reading process to flash memory and SRAM. Each chip select signals in the OM6359 select memory among 2 flash memory and SCRAM. Reading or writing procedure is processed after HWR_N or HRD_N is enabled. Memories use reset, which is VDD3 delay from PCF50601. HA[25] signal enables lower byte of SRAM and HA[26] signal enables higher byte of SRAM.

9. OM6359

OM6359 is consisted of ARM core and DSP core. It has 8x1Kword on-chip program/data RAM, 55 Kwords on-chip program ROM in the DSP. It has 4K*32bits ROM and 2K*32bits RAM in the ARM core. DSP is consisted of KBS, JTAG, EMI and UART. ARM core is consisted of EMI, PIC(Programmable Interrupt Controller), reset/power/clock unit, DMA controller, TIC(Test Interface Controller), peripheral bridge, PPI, SSI(Synchronous Serial Interface), ACC(Asynchronous communications controllers), timer, ADC, RTC(Real-Time Clock) and keyboard interface. KBIO(0:7), address lines of DSP core and HD[0~15]. HA[1~26], address lines of ARM core and HD[0~15], data lines of ARM core are connected to memory, YMU762C. MV317S(Camera DSP Chip) controls the communication between ARM core and DSP core.

CS_NAND, NCSRAM, NCSFLASH in the ARM core are connected to each memory. HWR_N and HRD_N control the process of memory. External IRQ(Interrupt ReQuest) signals from each units, such as, PMU need the compatible process. KBIO[0~7] receive the status from key and RXD0/TXD0 are used for the communication using data link cable(DEBUG_DTR/RTS/TXD/RXD/CTS/DSR).

It has JTAG control pins(TDI/TDO/TCK) for ARM core and DSP core. It receives 13MHz clock in CKI pin from external TCXO. ADC(Analog to Digital Convertor) part receives the status of temperature, battery type and battery voltage.

10. TOH2600DGI4KRA(26MHz)

This system uses the 26MHz TCXO, TOH2600DGI4KRA, SEM. AFC control signal from OM6359 controls frequency from 26MHz x-tal. The clock output frequency of UAA3536 is 13MHz. This clock is connected to OM6359, YMU762C.

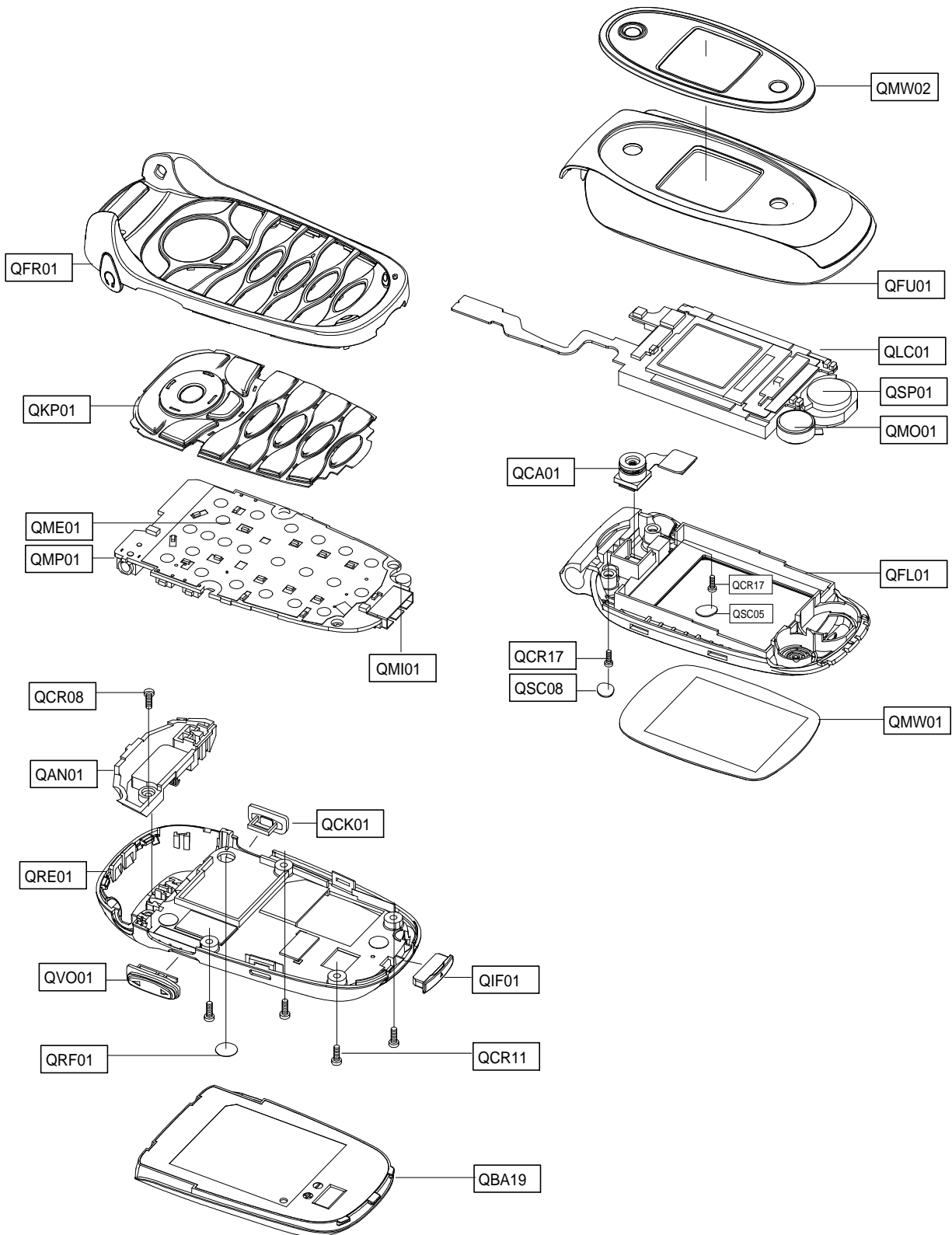
11. Camera DSP(MV317S)

Tiger is an Integrated circuit for mobile phone camera. This structure will allow effectiveness for large data management and significantly reduces main processor will get burden.

In hence, Tiger will allow the user to be able to display to LCD direct without burdening the main processor. It also allows to have various kinds of display size on the LCD and snapshot for Jpeg. Digital effect will also be executed on real time base resulting Tiger as being a video co-processor in the mobile platform. Also, an i80 type processor's 16bit parallel interface of Tiger makes it available for the CPU to interchange the data with Tiger. As the additional 8Mbit is usable except 2Mbit buffer embedded in Tiger, the diverse UI data processing which is not a burden to the CPU is available. JPEG encoder and decoder are baseline ISO/IEC 10918-1 JPEG compliance (DCT-based). JPEG decoder supports YUV444, YUV422, YUV420 and YUV411 format standard JPEG image.

3. SGH-E330 Exploded View and its Parts list

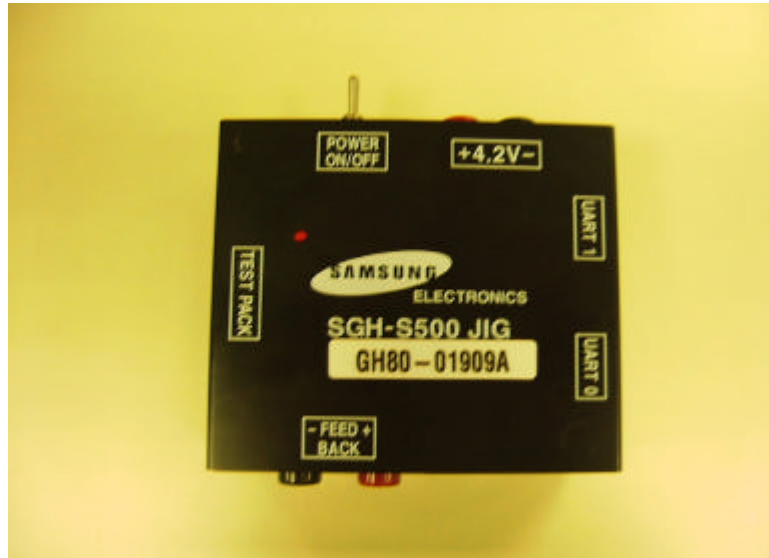
1. Cellular phone Exploded View - 1



2. Cellular phone Parts list

Location NO.	Description	SEC CODE	Remark
QMW02	SUB WINDOW	GH75-04905A	
QFU01	FOLDER UPPER	GH75-04615A	
QSP01	SPEAKER	3001-001598	
QM001	MOTOR DC	3101-001401	
QLC01	LCD	GH07-00593A	
QCA01	UNIT CAMERA	GH59-01472A	
QCR17	SCREW	6001-001639	
QSC05	SCREW SHEET R	GH74-08872A	
QSC08	SCREW SHEET L	GH74-08873A	
QFL01	FOLDER LOWER	GH75-04618A	
QMW01	MAIN WINDOW LCD	GH75-04904A	
QFR01	FRONT COVER	GH75-04616A	
QKP01	KEKPAD	GH75-04619A	
QMP01	PBA MAIN	GH92-01844A	
QMI01	MICROPHONE ASSY	GH30-00130A	
QME01	UNIT METAL DOM	GH59-01547A	
QCR08	SCREW	6001-001456	
QAN01	ANTENNA	GH42-00454A	
QRE01	REAR COVER	GH75-04617A	
QCR11	SCREW	6001-001654	
QV001	VOLUME KEY	GH72-13531A	
QCK01	CAMERA KEY	GH72-13532A	
QIF01	IF COVER	GH72-13534A	
QRF01	RF SHEET	GH74-09328A	
QBA19	BATTERY	GH43-01398A	

3. Test Jig (GH80-01909A)



3-1. RF Test Cable
(GH39-00283A)



3-2. Test Cable
(GH39-00217A)



3-3. Serial Cable



3-4. Power Supply Cable



3-5. DATA CABLE
(GH39-00219A)



3-6. TA
(GH44-00482A)



4. SGH-E330 MAIN Electrical Parts List

SEC Code	Design LOC
0403-001387	ZD502
0403-001427	ZD501
0404-001089	ZD500
0406-001194	ZD600
0406-001194	ZD601
0406-001194	ZD700
0406-001194	ZD701
0406-001201	D700
0406-001201	D701
0504-001012	Q500
0504-001012	Q600
0505-001423	U701
0506-000107	Q700
0601-001790	LED700
0601-001790	LED701
0601-001790	LED702
0601-001790	LED703
0601-001790	LED704
0601-001790	LED705
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0601-001790	LED708
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0601-001790	LED711
0601-001790	LED712
0601-001790	LED713
0601-001790	LED714
0801-002237	U300
0801-002882	U201
0801-002882	U304
0801-002882	U306
1001-001253	U603
1009-001018	SW600
1109-001316	U302
1201-002174	U102
1202-001036	U610
1203-003459	U702
1203-003483	U501

SEC Code	Design LOC
1203-003486	U502
1204-002161	U301
1205-002327	U100
1205-002350	U400
1205-002607	U200
1404-001221	TH200
1405-001082	V600
1405-001082	V601
1405-001082	V602
1405-001082	V603
1405-001082	V604
1405-001082	V605
1405-001128	V700
1405-001128	V702
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2007-000142	R121
2007-000143	R700
2007-000143	R701
2007-000147	R129
2007-000148	R110
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2007-000148	R400
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2007-000148	R607
2007-000153	R304

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2007-000171	R718
2007-000172	R212
2007-000172	R213
2007-000174	R606
2007-000242	R605
2007-000566	R103
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2007-000775	R118
2007-001288	R124
2007-001298	R104
2007-001301	R703
2007-001301	R704

SEC Code	Design LOC
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2007-001305	R115
2007-001308	R114
2007-001313	R125
2007-001313	R126
2007-001313	R301
2007-001319	R306
2007-001325	R303
2007-001325	R402
2007-001341	R504
2007-002796	R611
2007-003029	R506
2007-007001	R208
2007-007001	R308
2007-007013	R307
2007-007014	R300
2007-007014	R302
2007-007100	R318
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2007-007107	R202
2007-007107	R204
2007-007142	R105
2007-007142	R203

Electrical Parts List

SEC Code	Design LOC
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2007-007148	R100
2007-007311	R106
2007-007314	R128
2007-007317	R511
2007-007334	R509
2007-007334	R608
2007-007334	R610
2007-007489	R615
2007-007528	R102
2007-007573	R507
2007-007588	R512
2007-007981	R614
2007-008117	R112
2007-008337	R502
2007-008672	R719
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2203-000604	C133
2203-000628	C608
2203-000679	C204
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2203-006208	C418
2203-006208	C419
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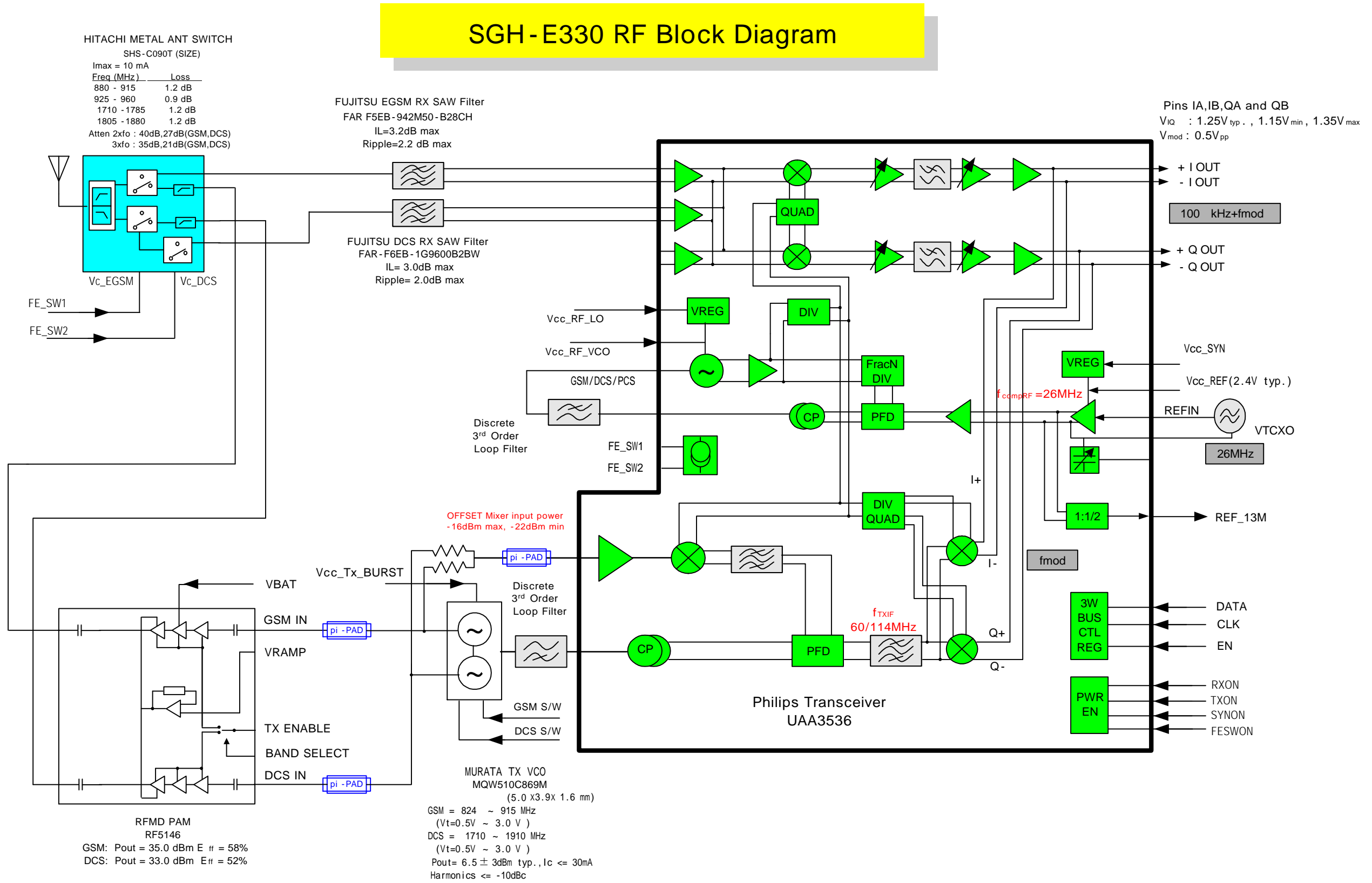
Electrical Parts List

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2404-001352	C627
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2703-001722	L107
2703-001723	L110
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2703-001723	L113
2703-001748	L106
2703-001970	L114
2703-002199	L105
2703-002203	L101
2703-002204	L109
2703-002208	L100
2703-002208	L102
2703-002267	L104
2703-002368	L111
2703-002779	L500
2801-004285	OSC300
2801-004339	X400
2806-001329	OSC101
2809-001281	OSC100
2901-001246	U500
2901-001254	F103
2901-001286	F700
2901-001286	F701
2901-001286	F702
2901-001286	F703
2901-001286	F704
2901-001286	F705
2904-001469	F100
2904-001470	F102
2904-001480	F101
2909-001246	U103
3301-001729	L620
3404-001152	SW300

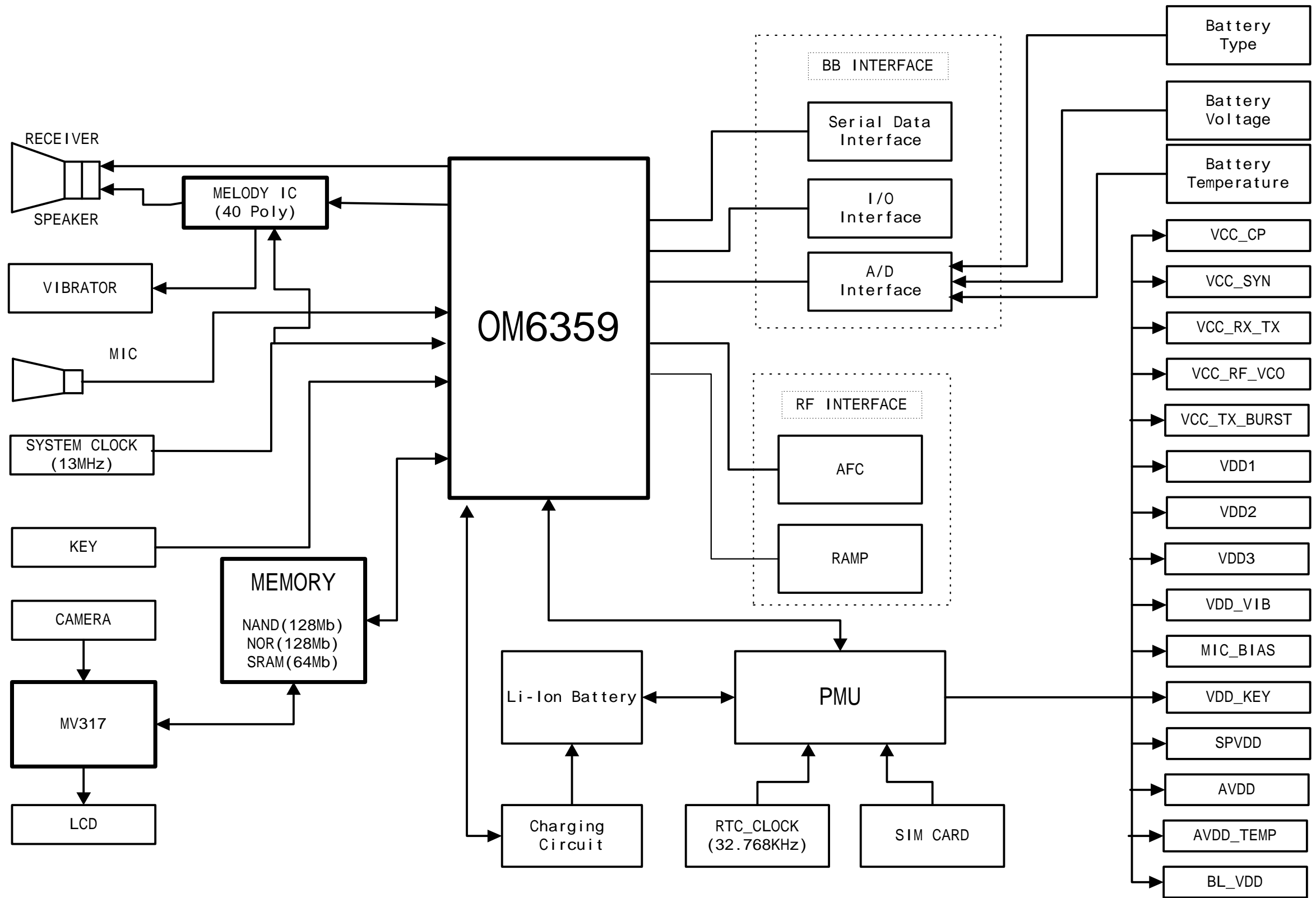
SEC Code	Design LOC
3404-001152	SW700
3404-001152	SW701
3705-001355	CON100
3709-001273	CN400
3710-001994	CN500
3711-005067	CN501
3711-005551	HDC700
3722-002249	EAR600
4302-001119	BAT400
GH13-00020A	U303
GH41-00627A	

5. SGH-E330 Block Diagrams

1. RF Solution Block Diagram



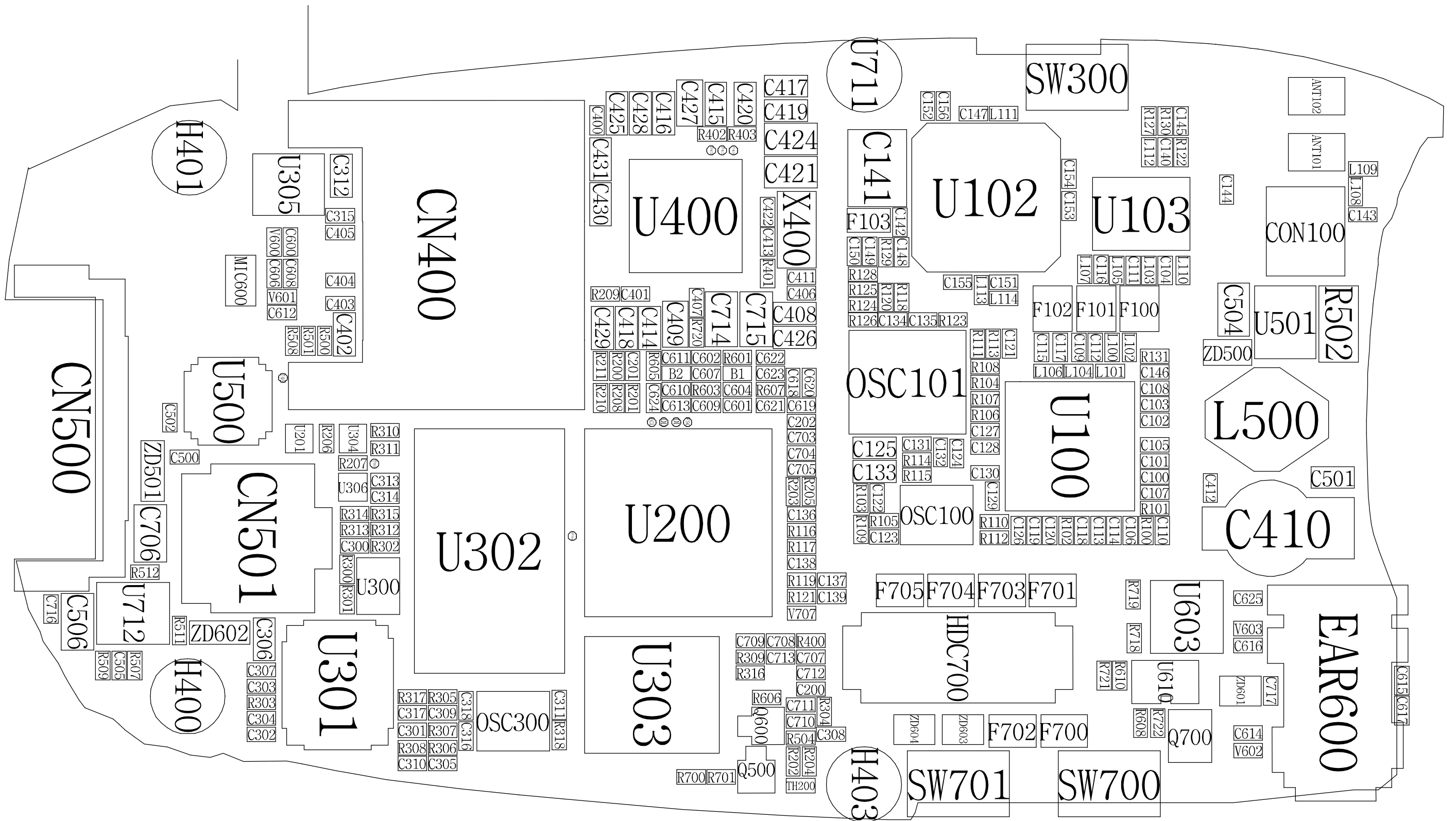
2. Base Band Solution Block Diagram



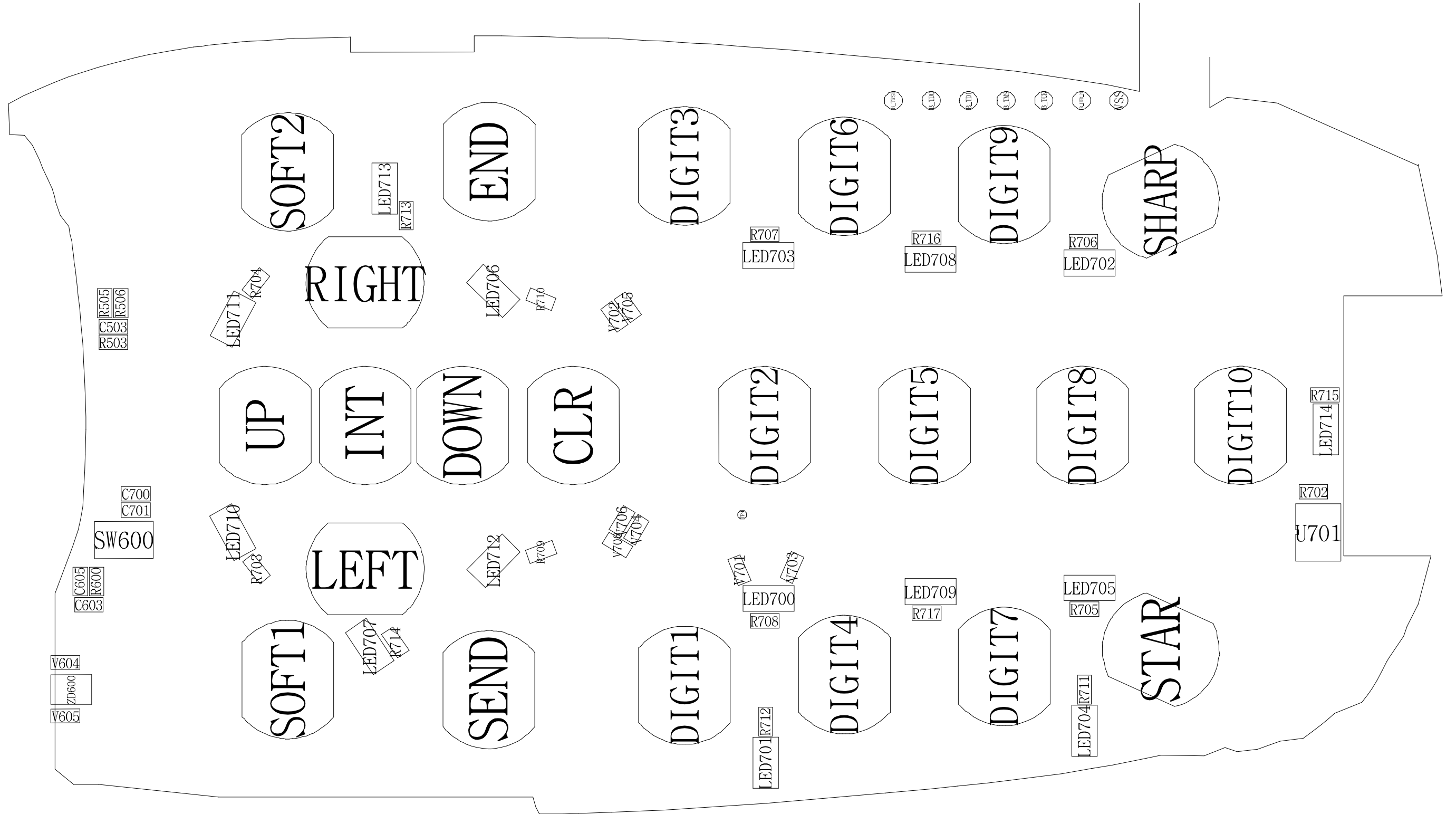
BB Block Diagram of SGH-E330

6. SGH-E330 PCB Diagrams

1. Main PCB Top Diagram

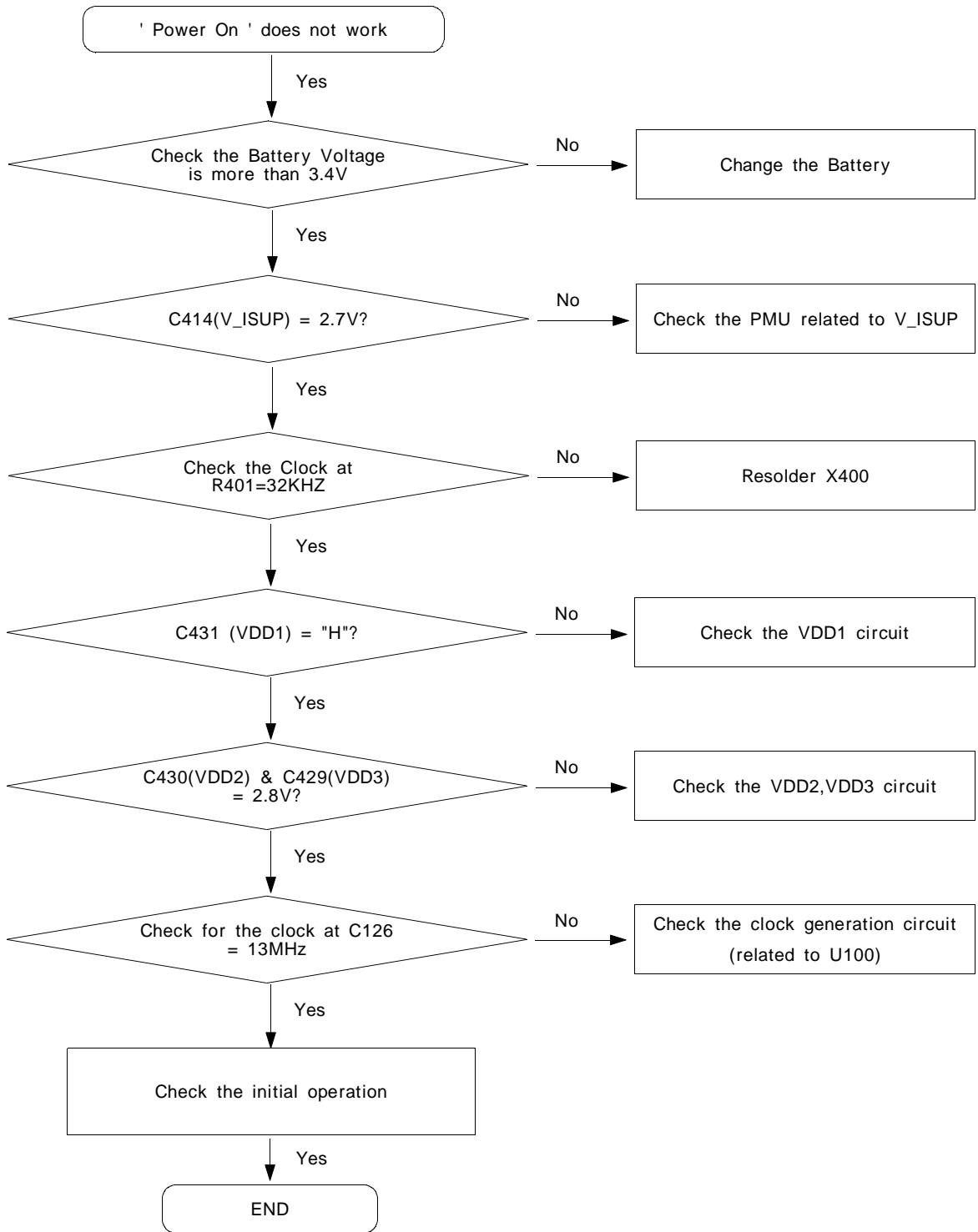


2. Main PCB Bottom Diagram

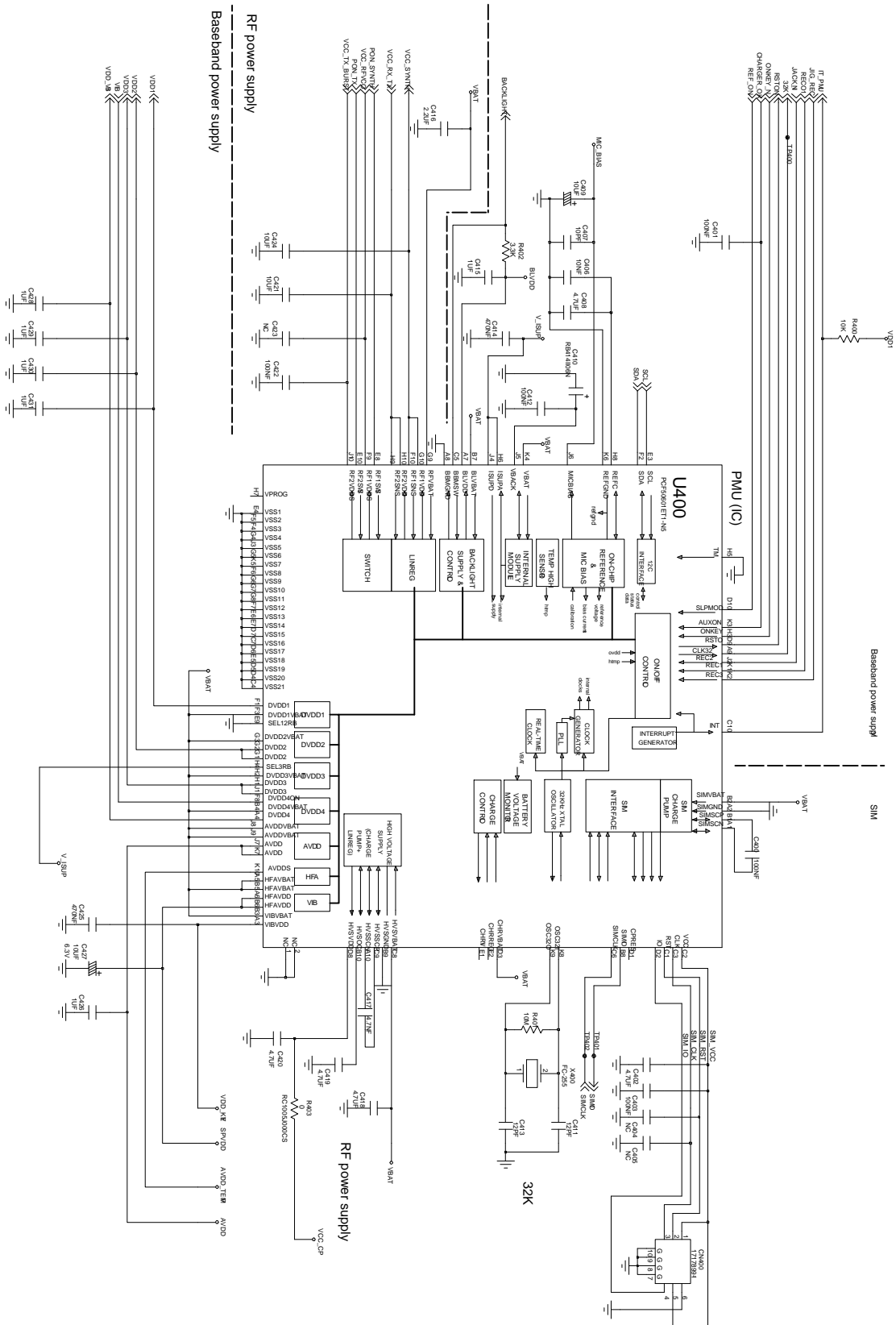


7. SGH-E330 Flow Chart of Troubleshooting

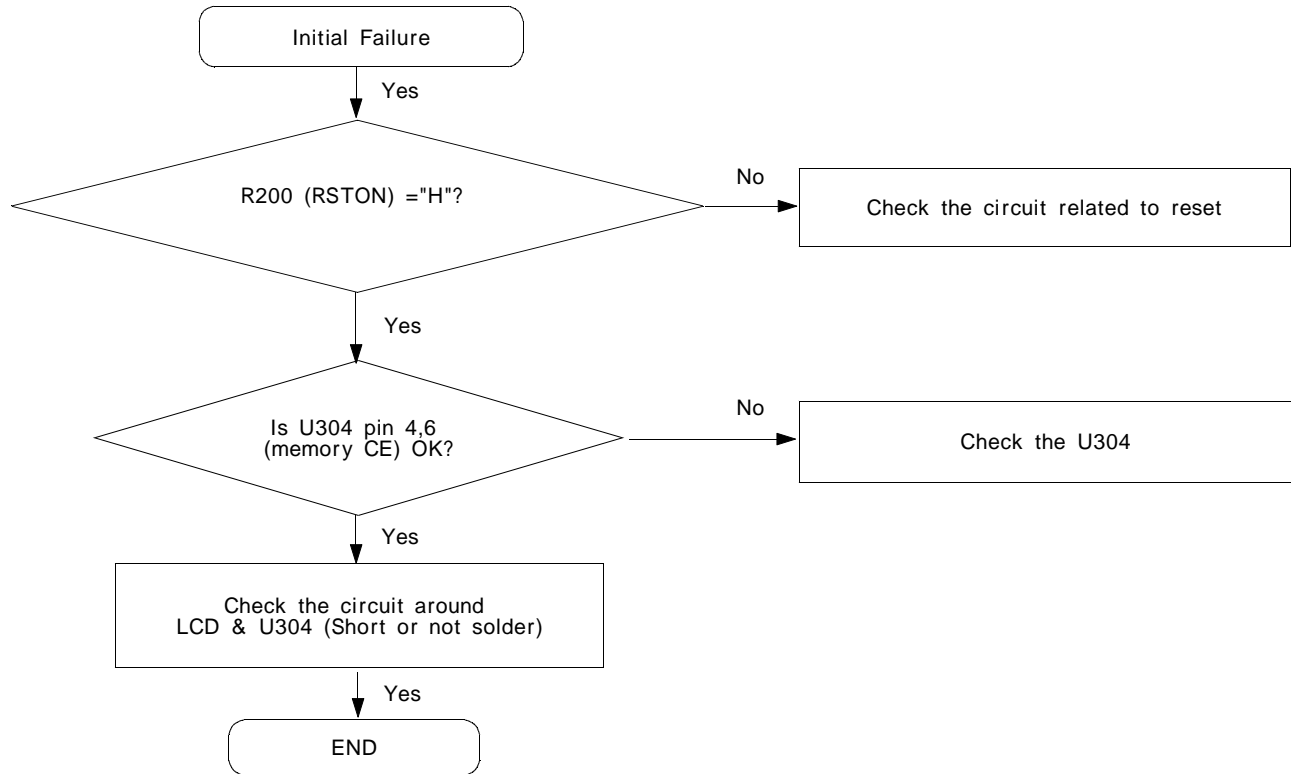
1. Power On



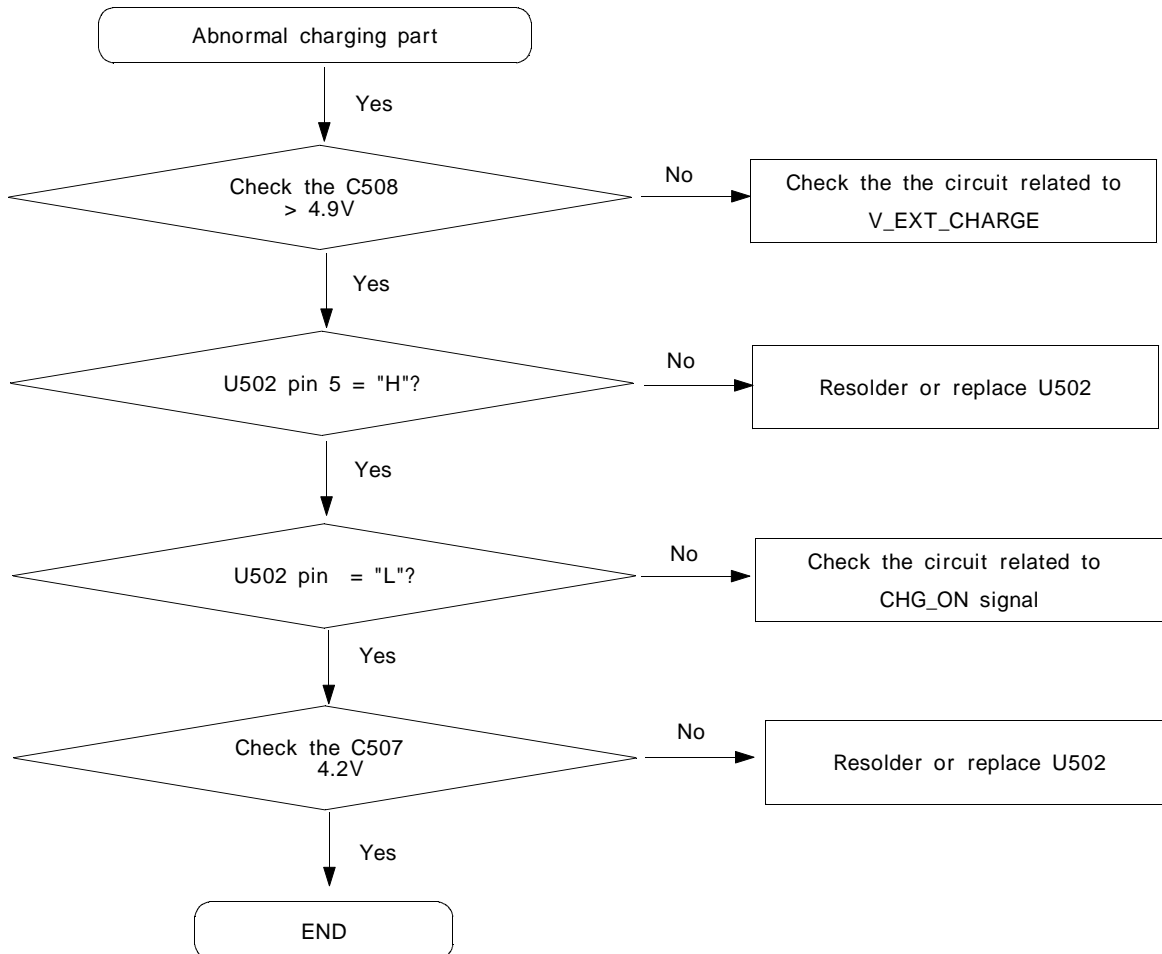
Power On



2. Initial

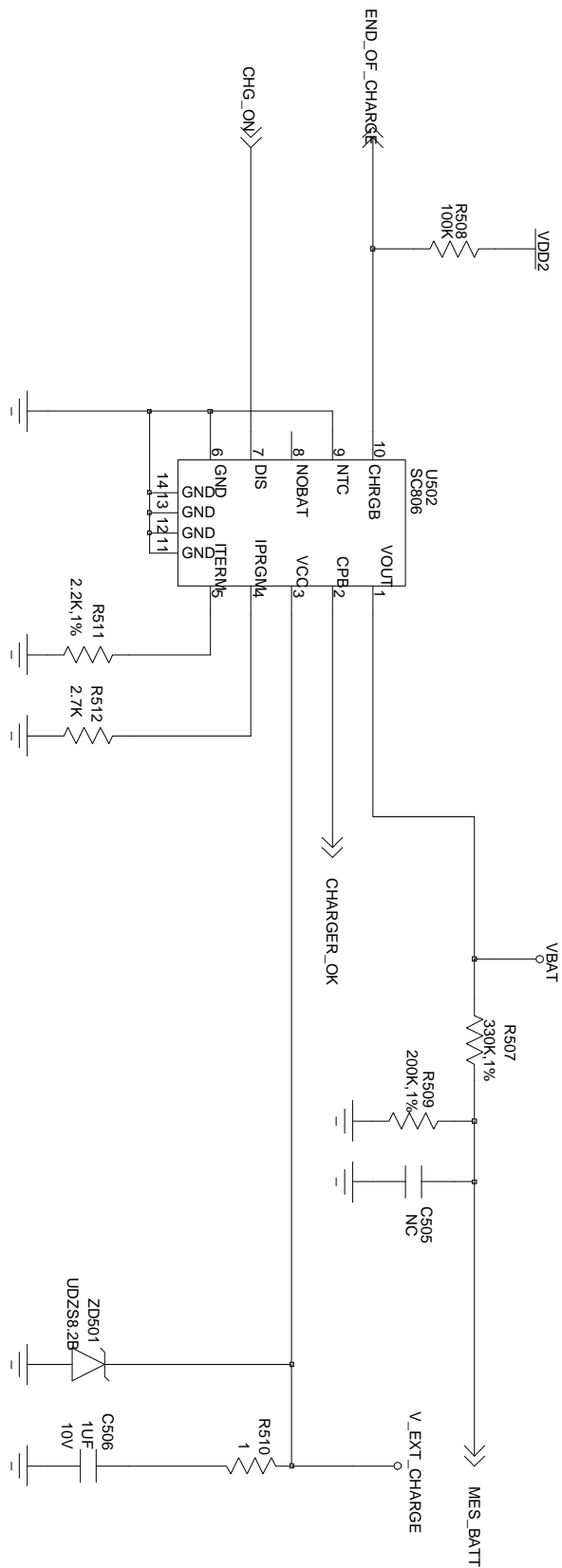


3. Charging Part

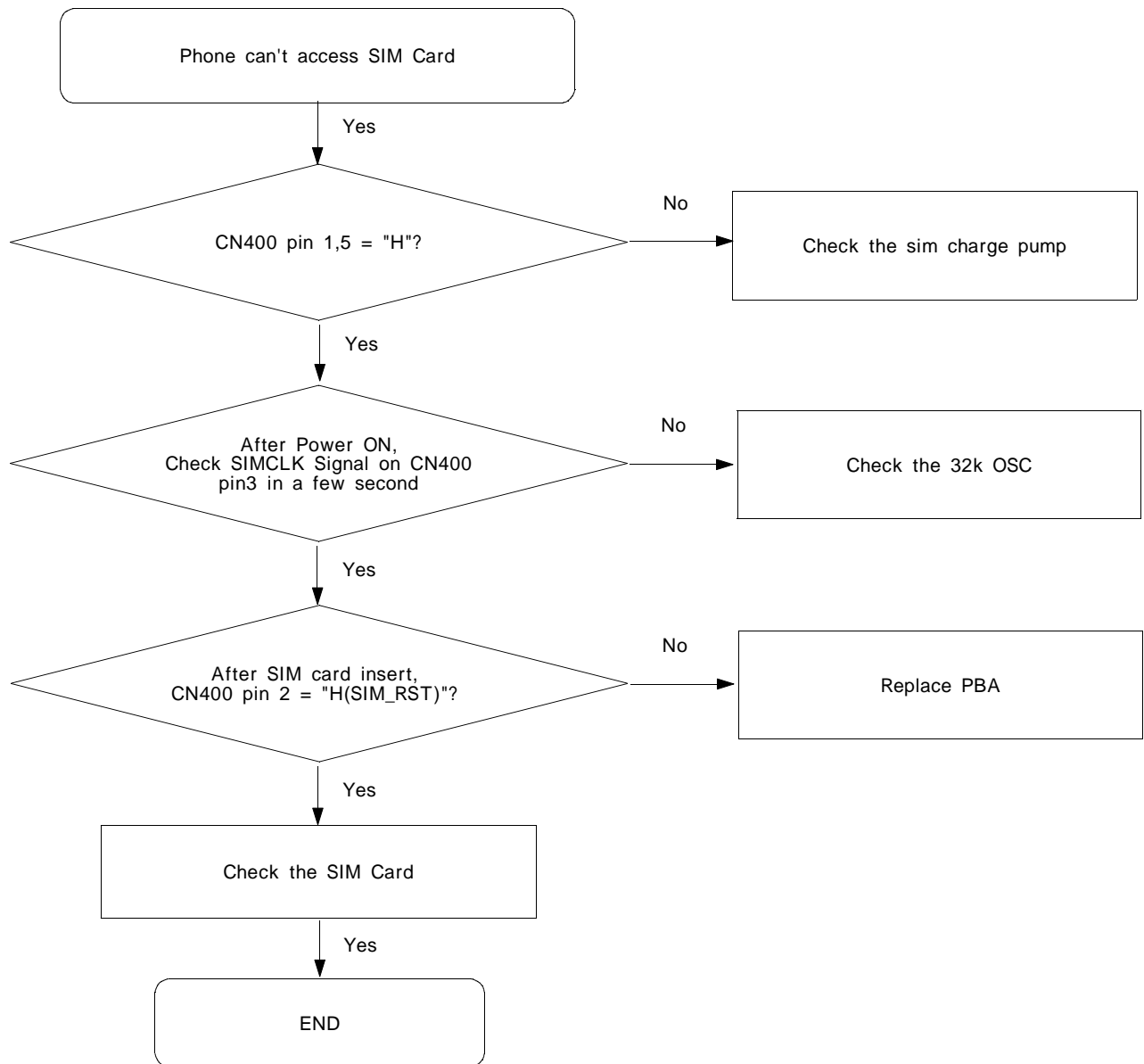


Charging

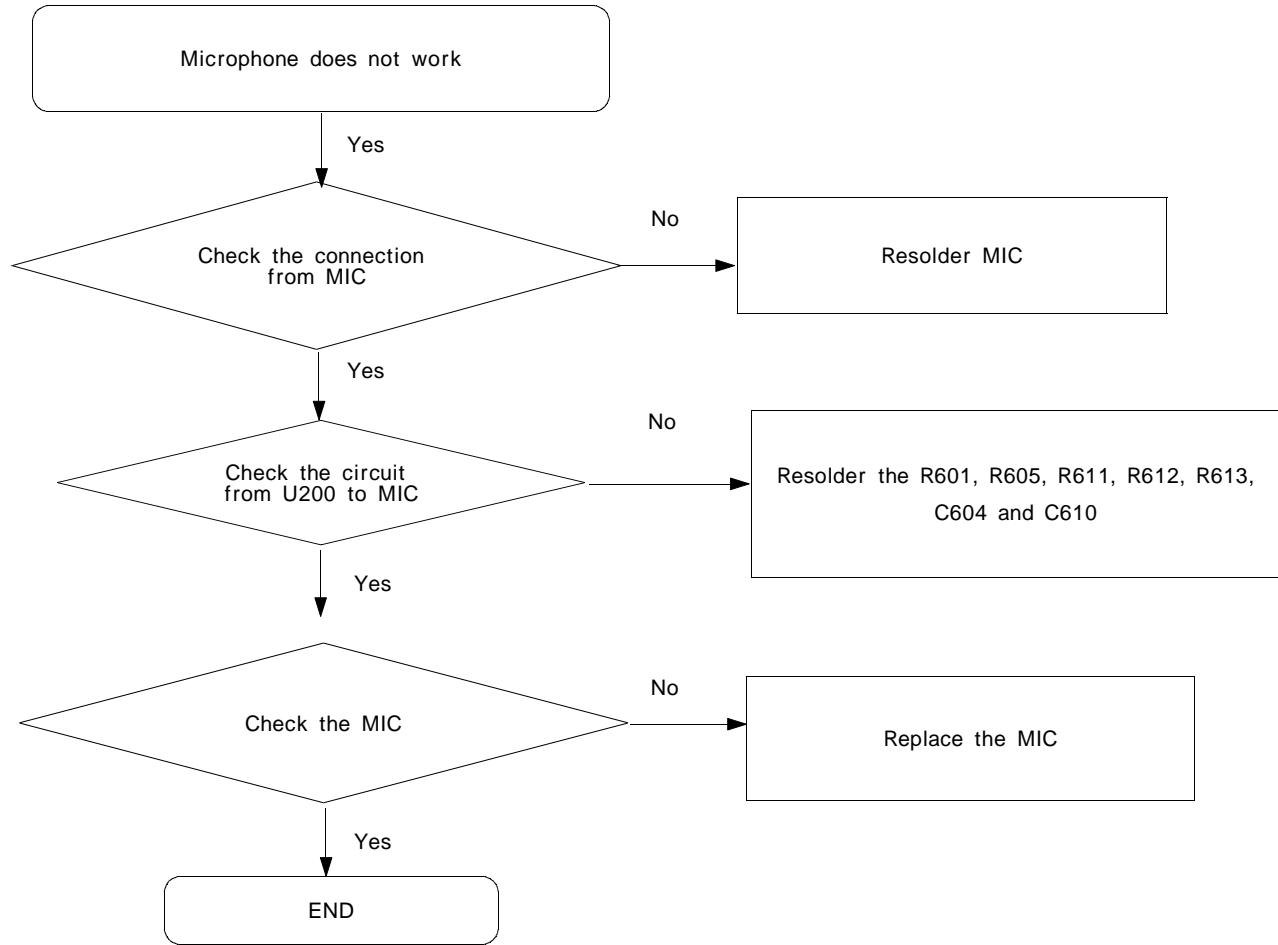
Charge of Battery



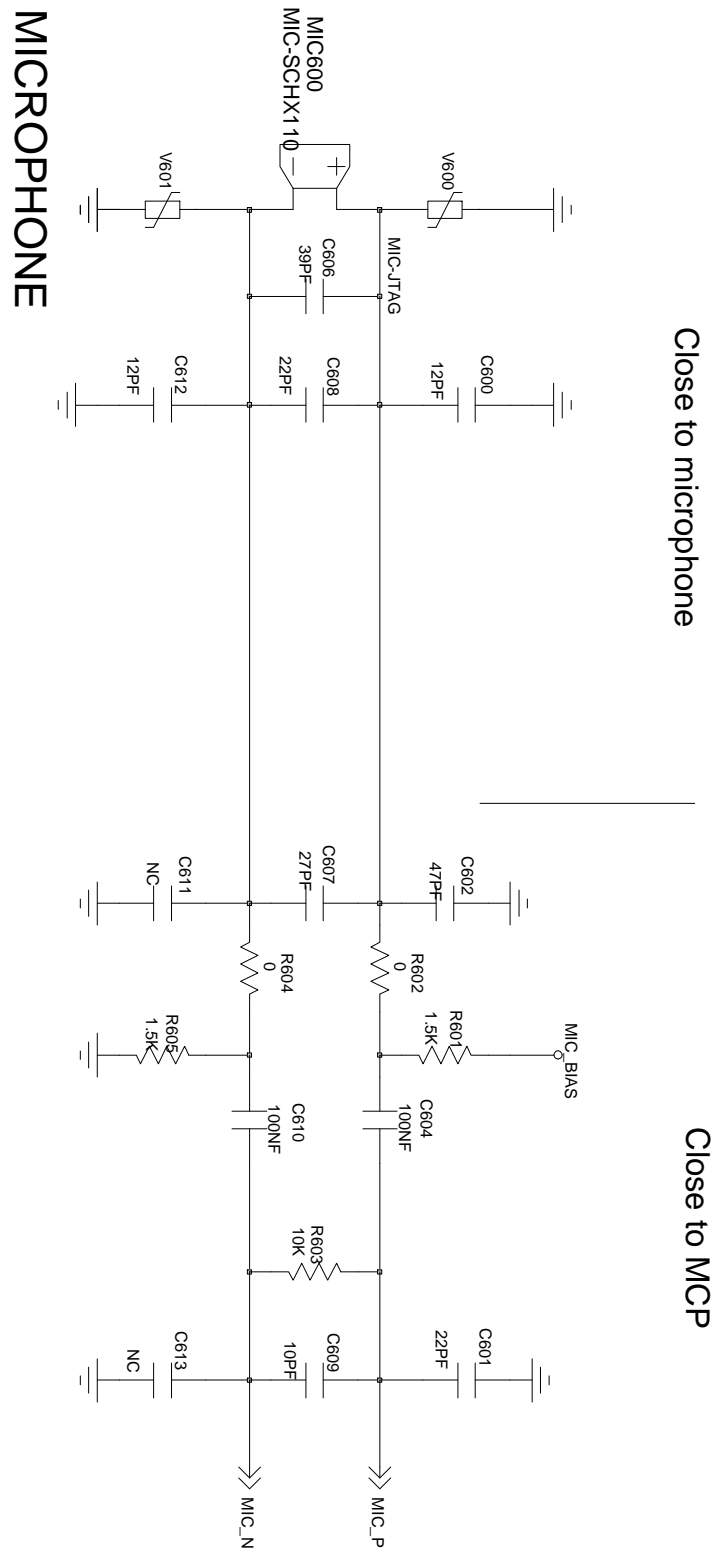
4. Sim Part



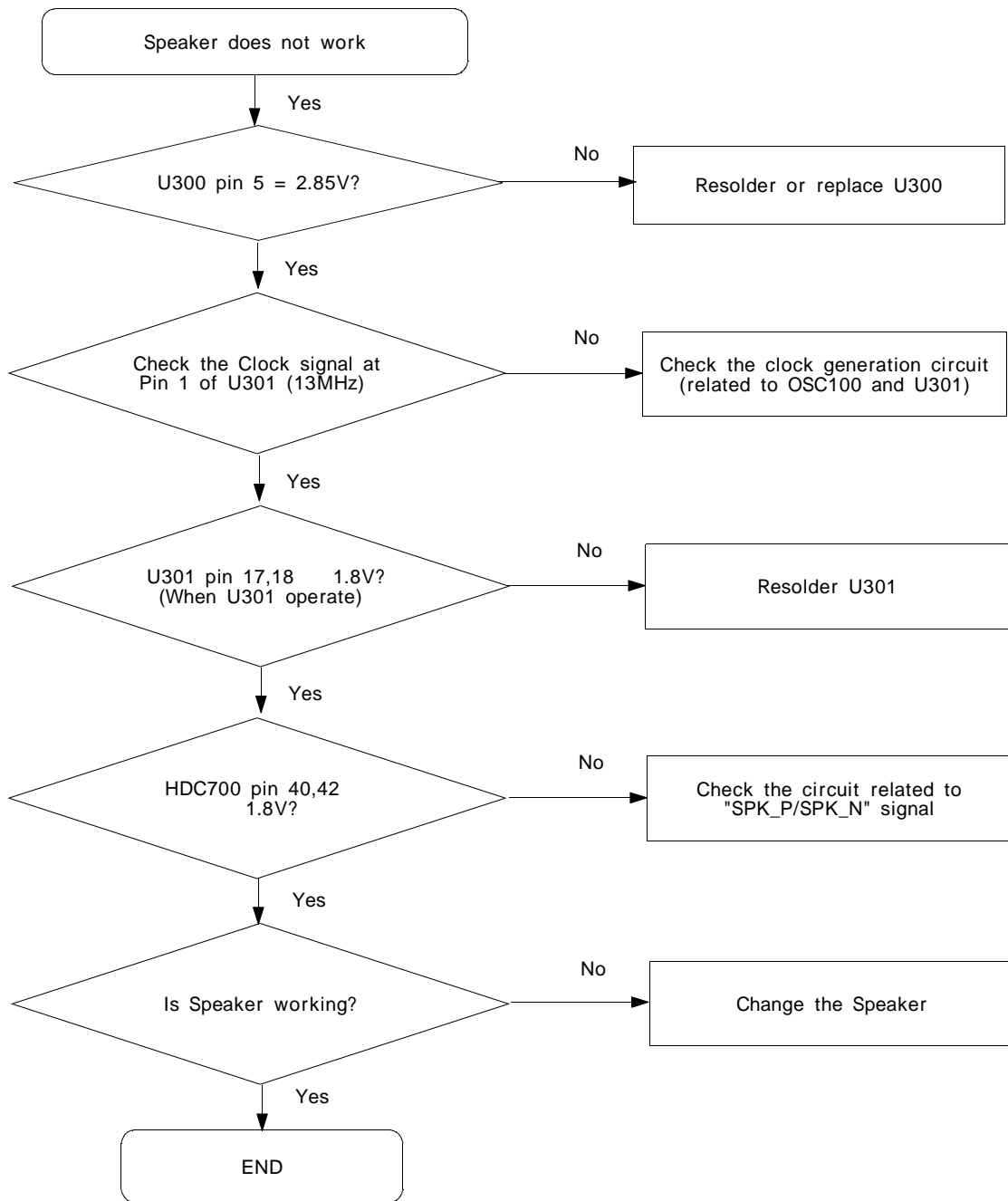
5. Microphone Part



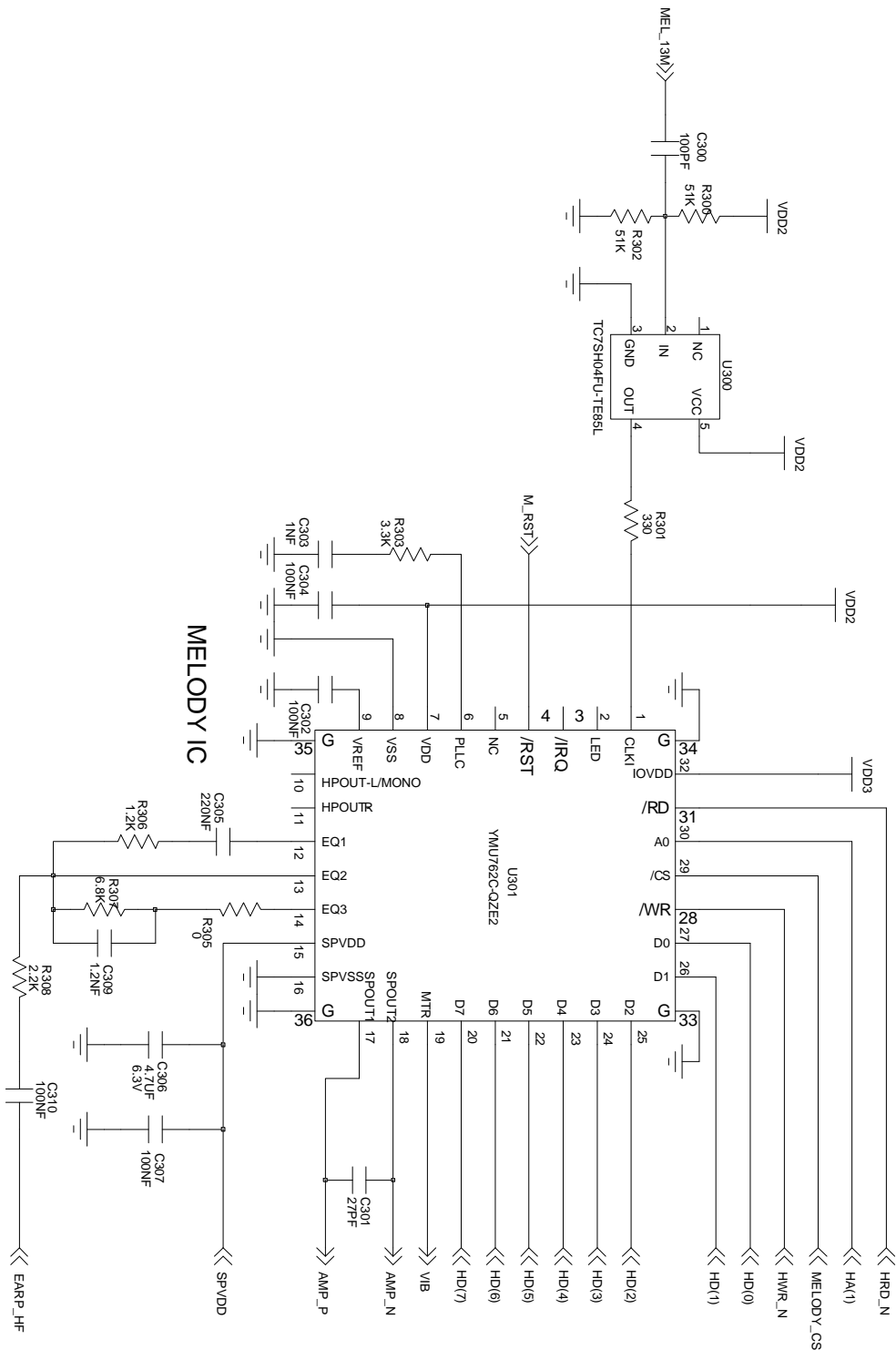
Microphone



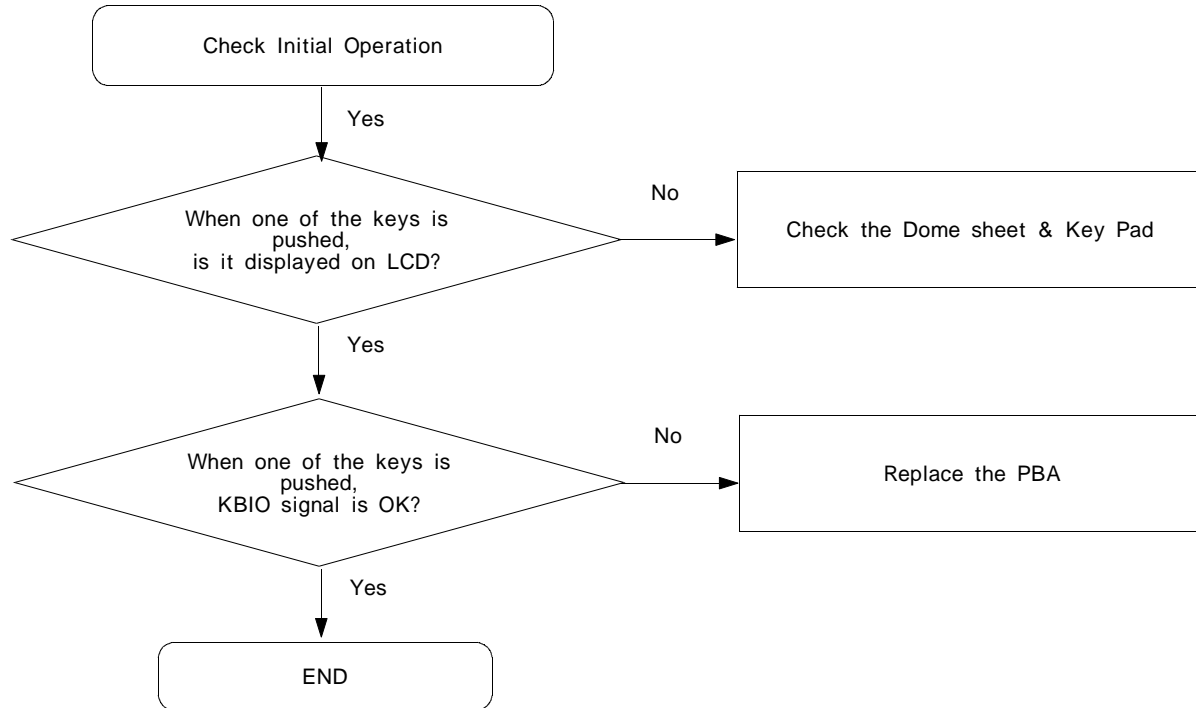
6. Speaker Part(Melody)



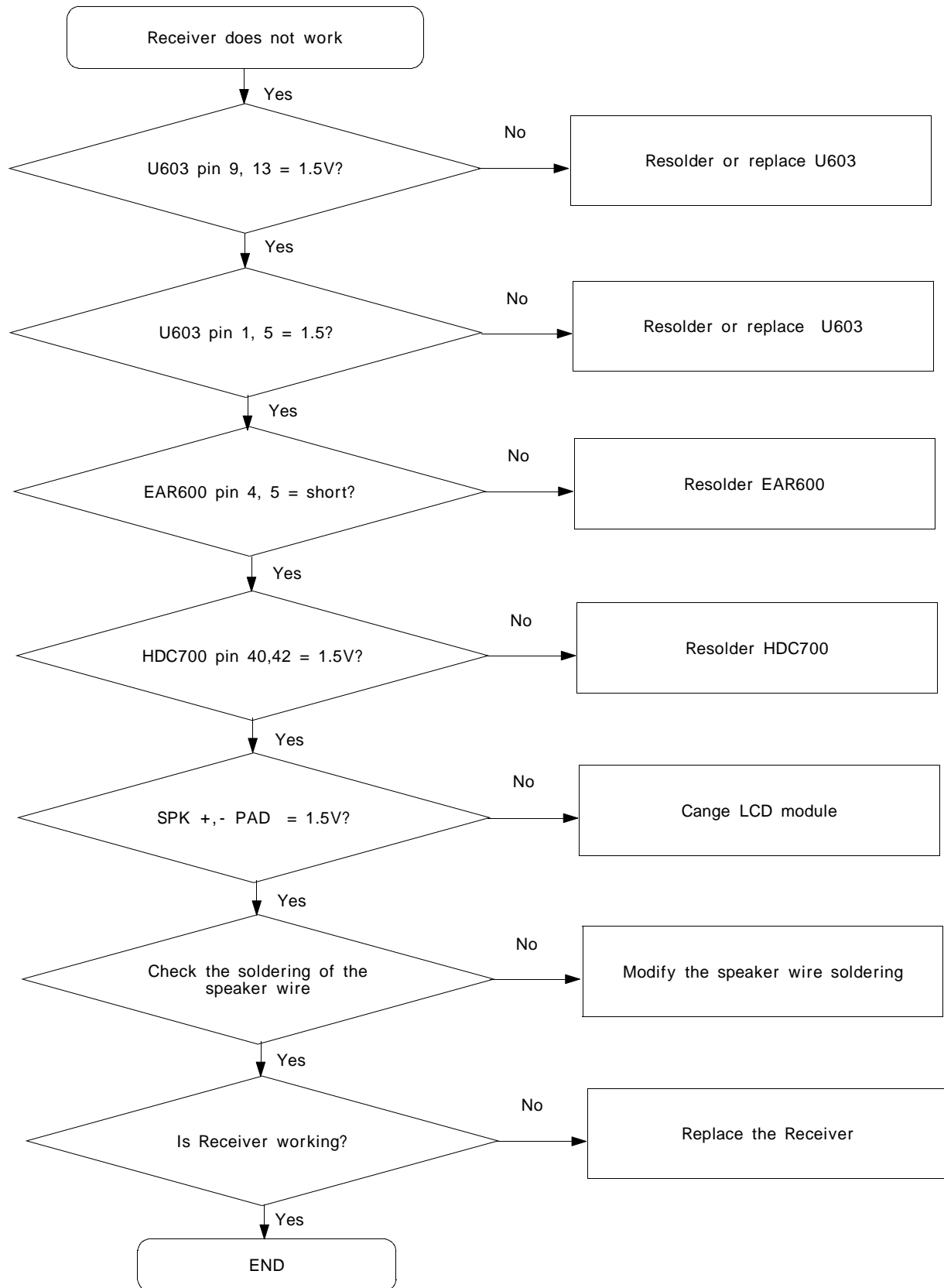
Speaker

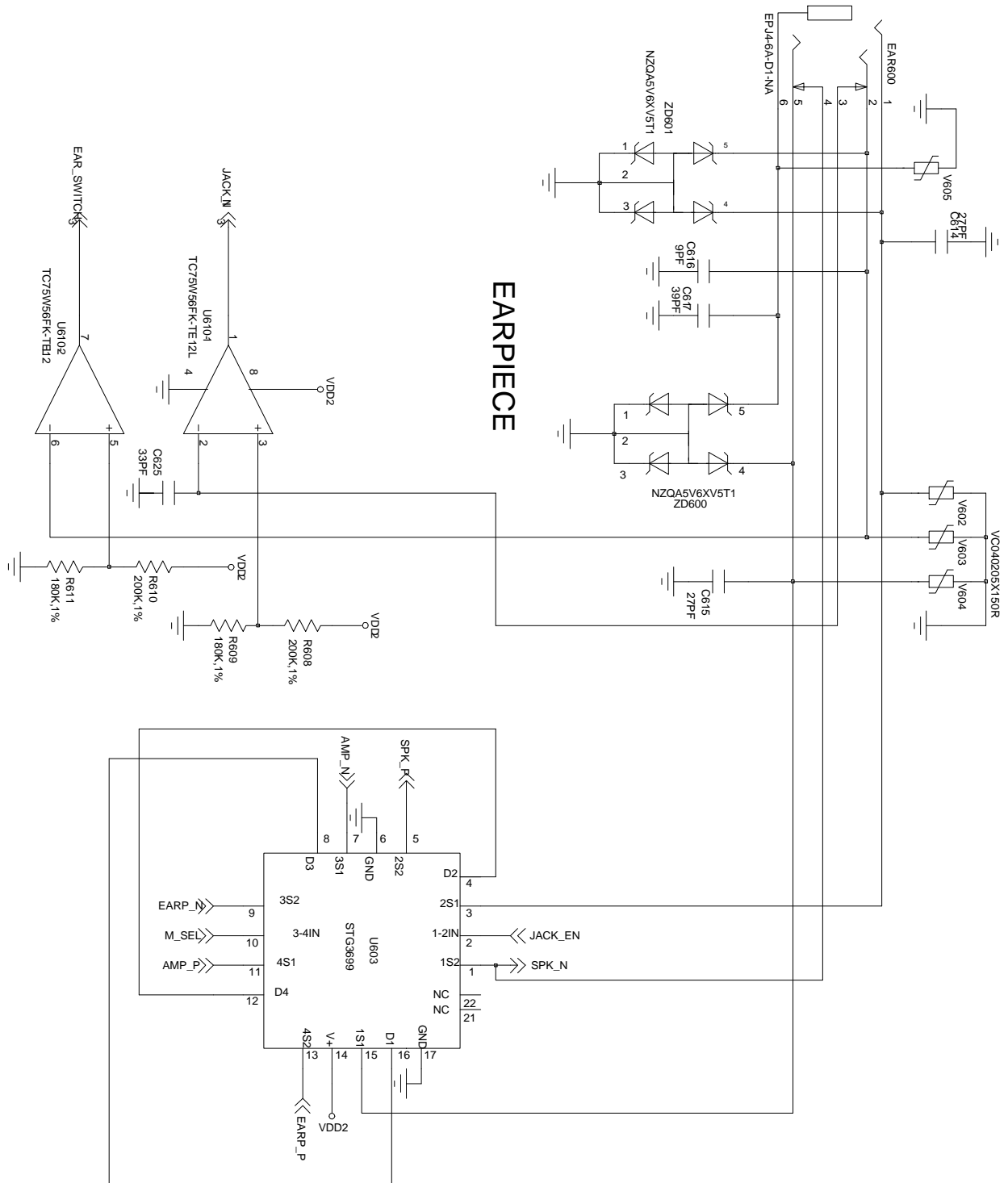


7. Key Data Input

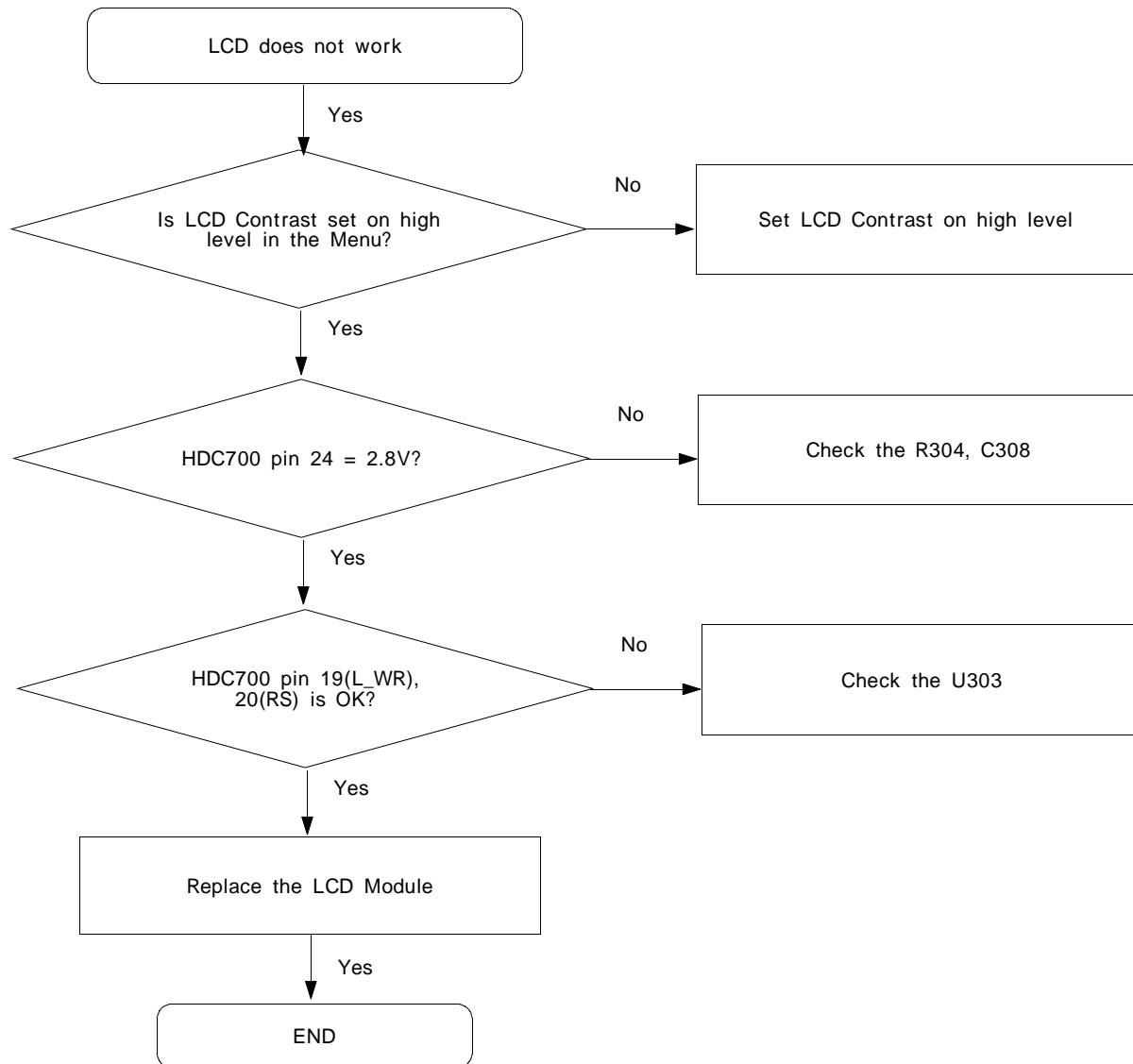


8. Receiver Part

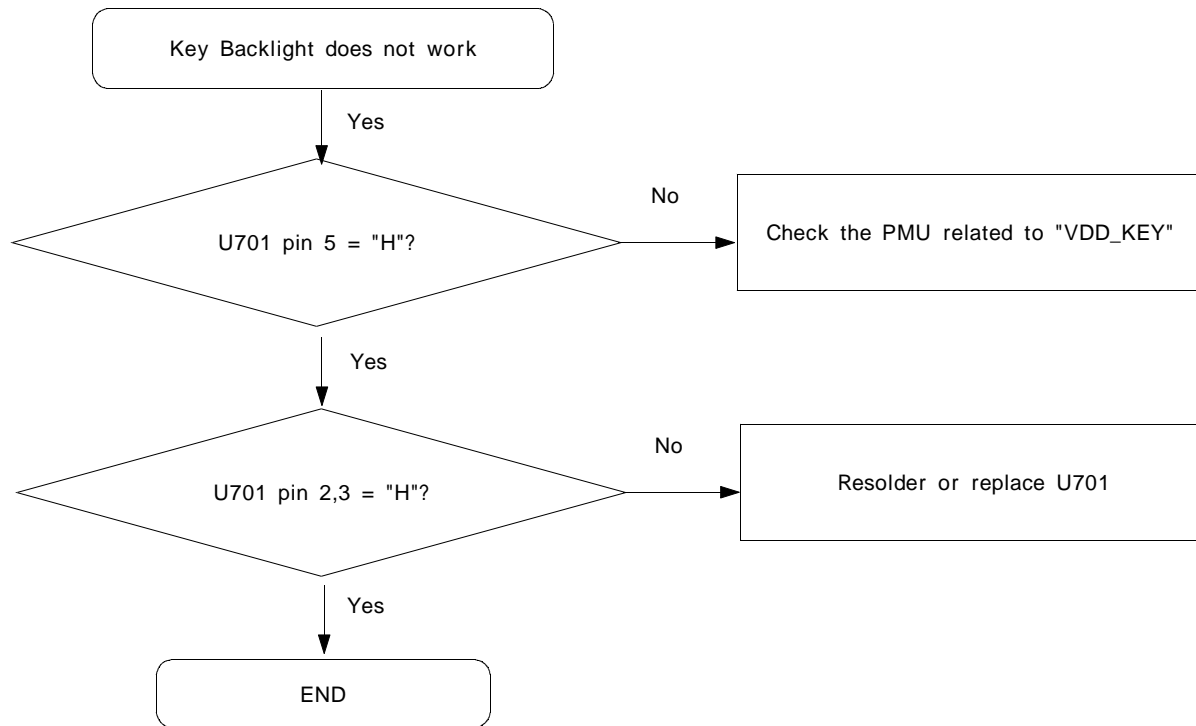




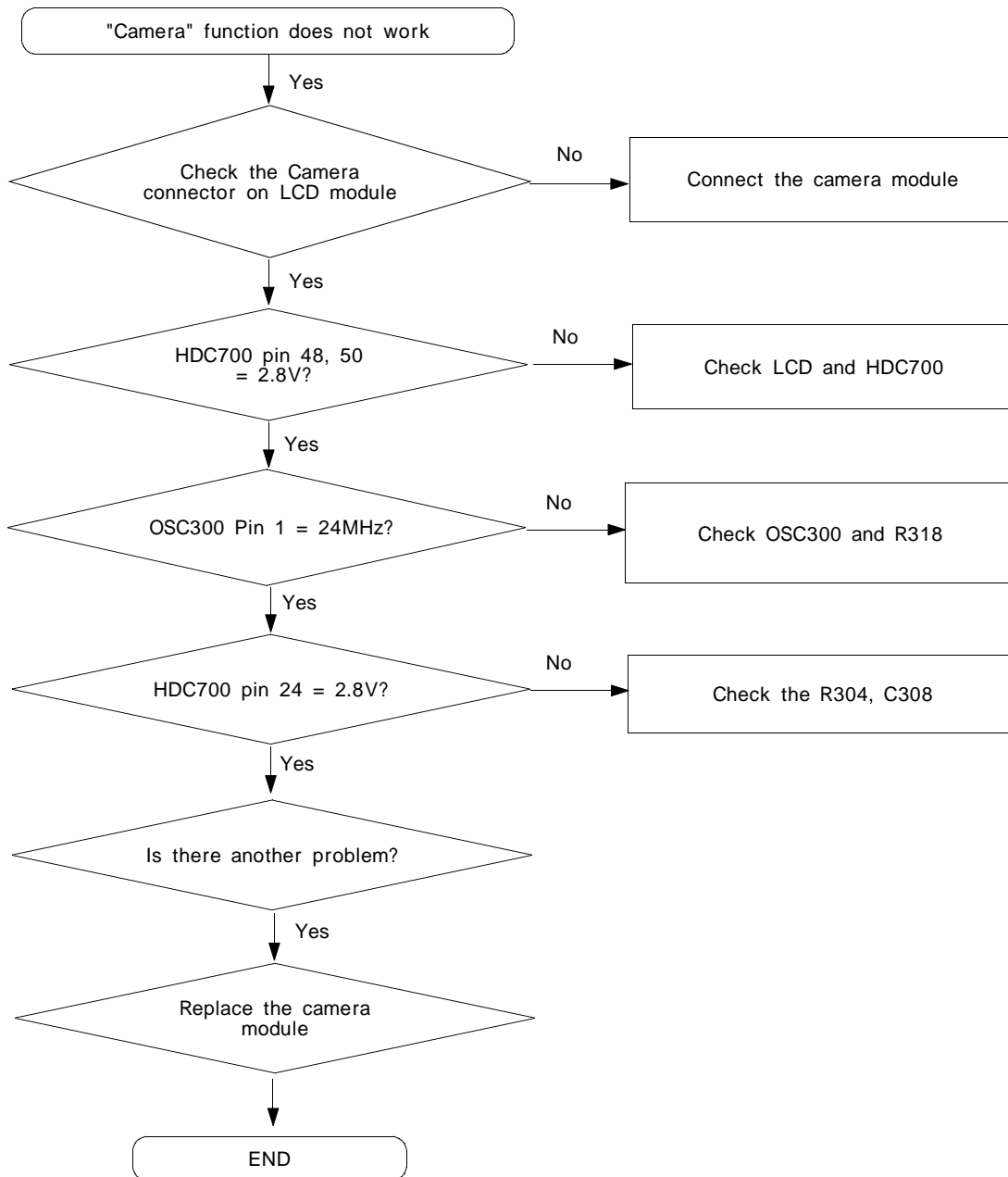
9. LCD Part

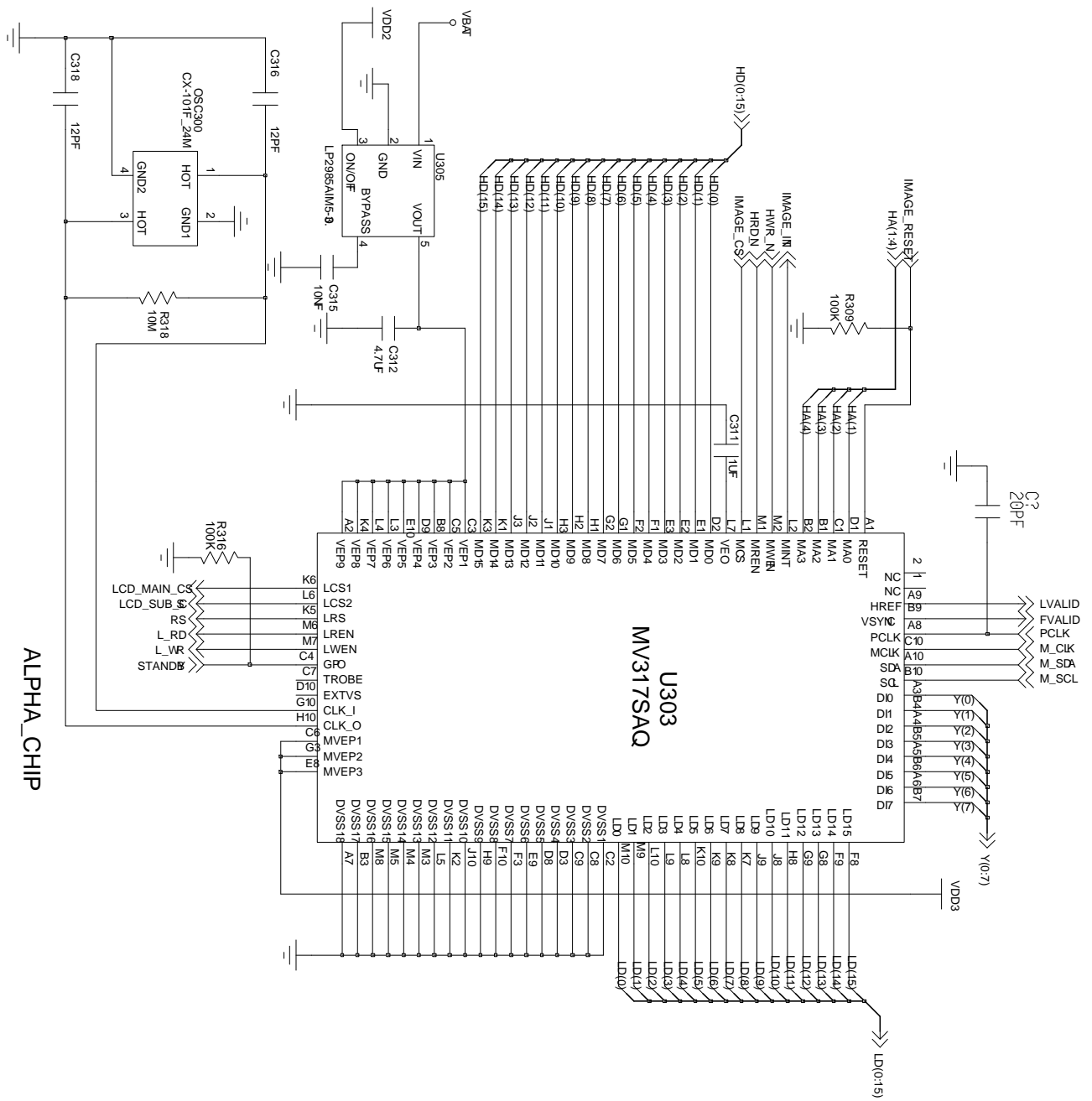


10. Key Back Light

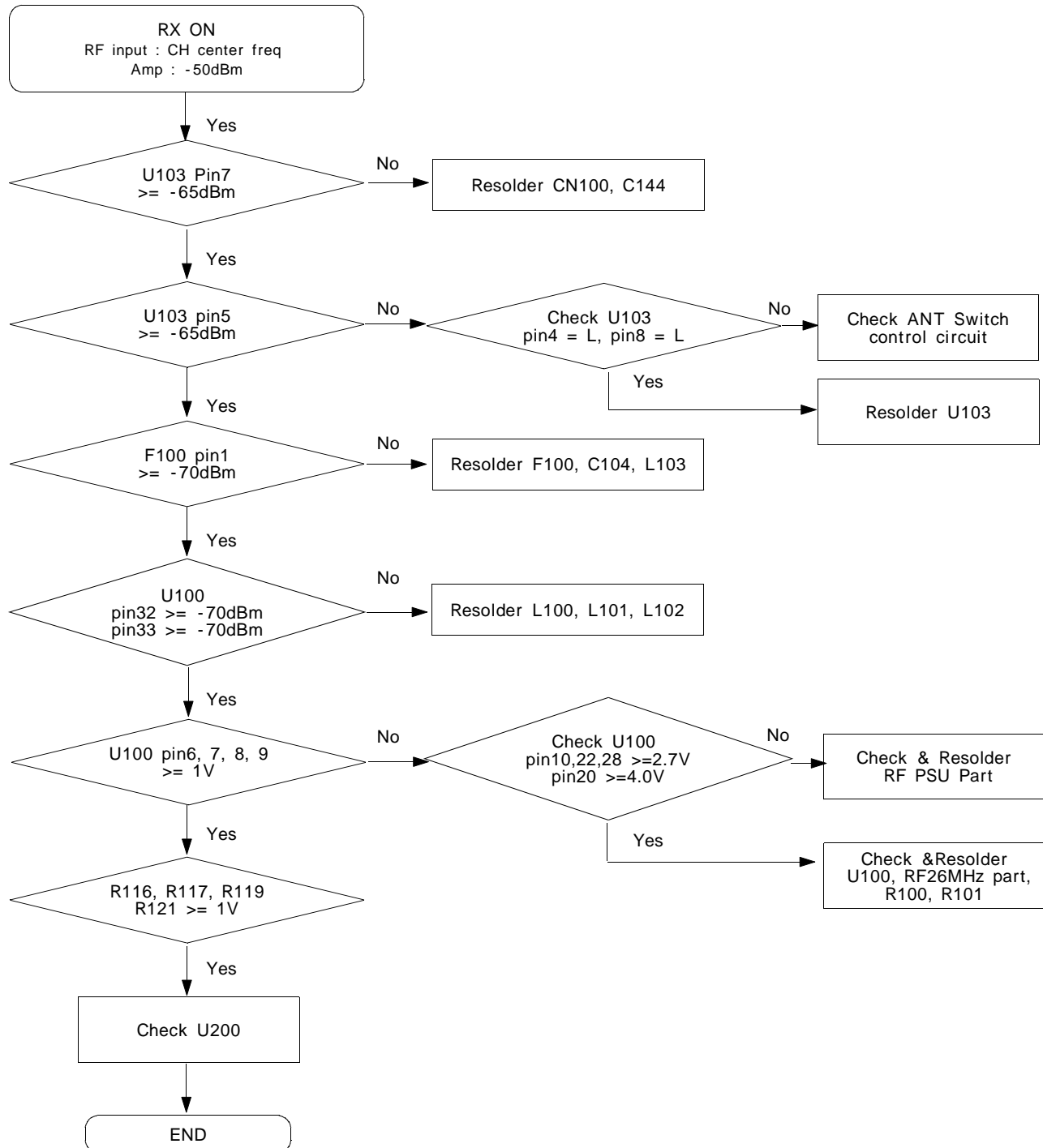


11. Camera part

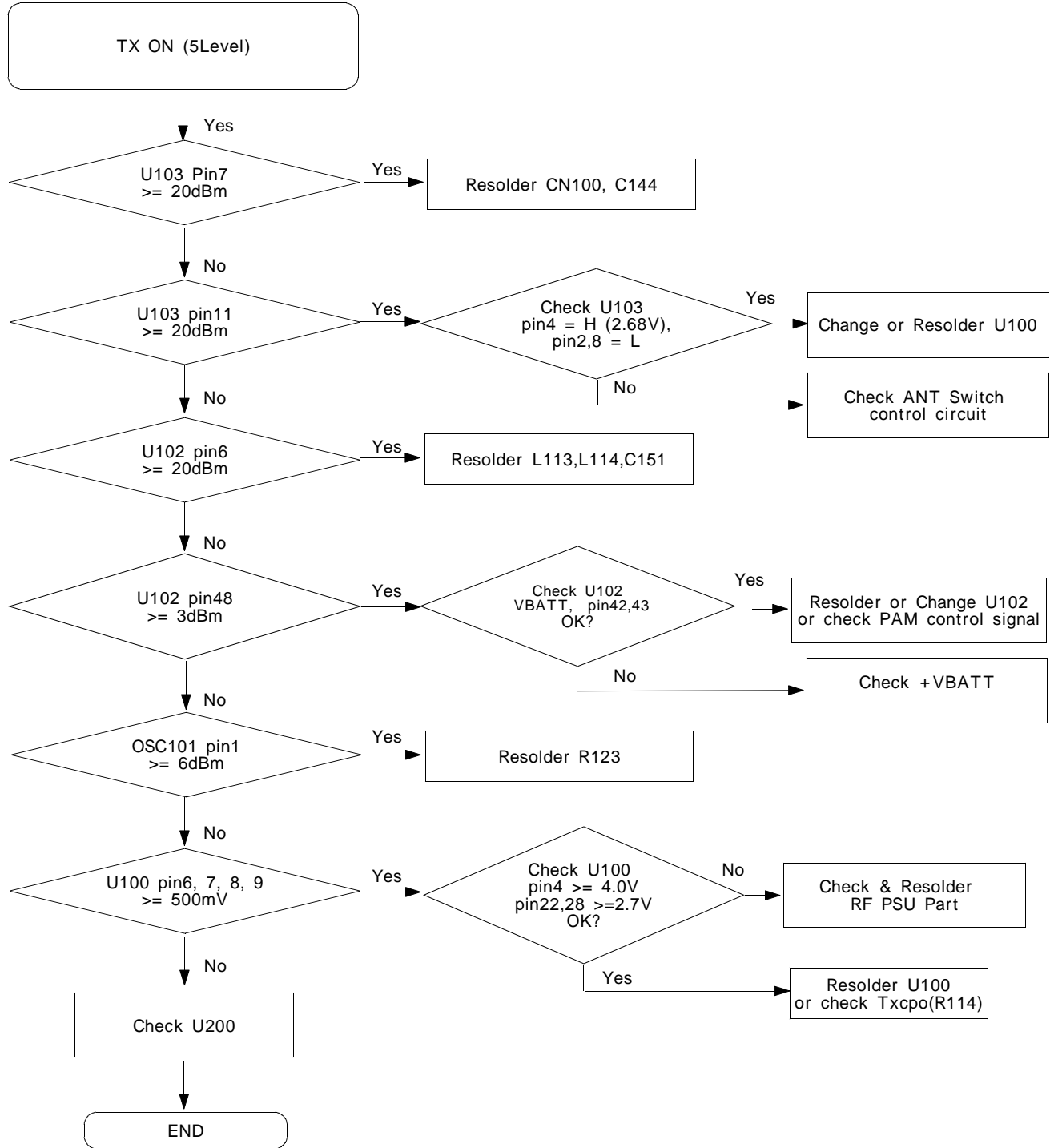




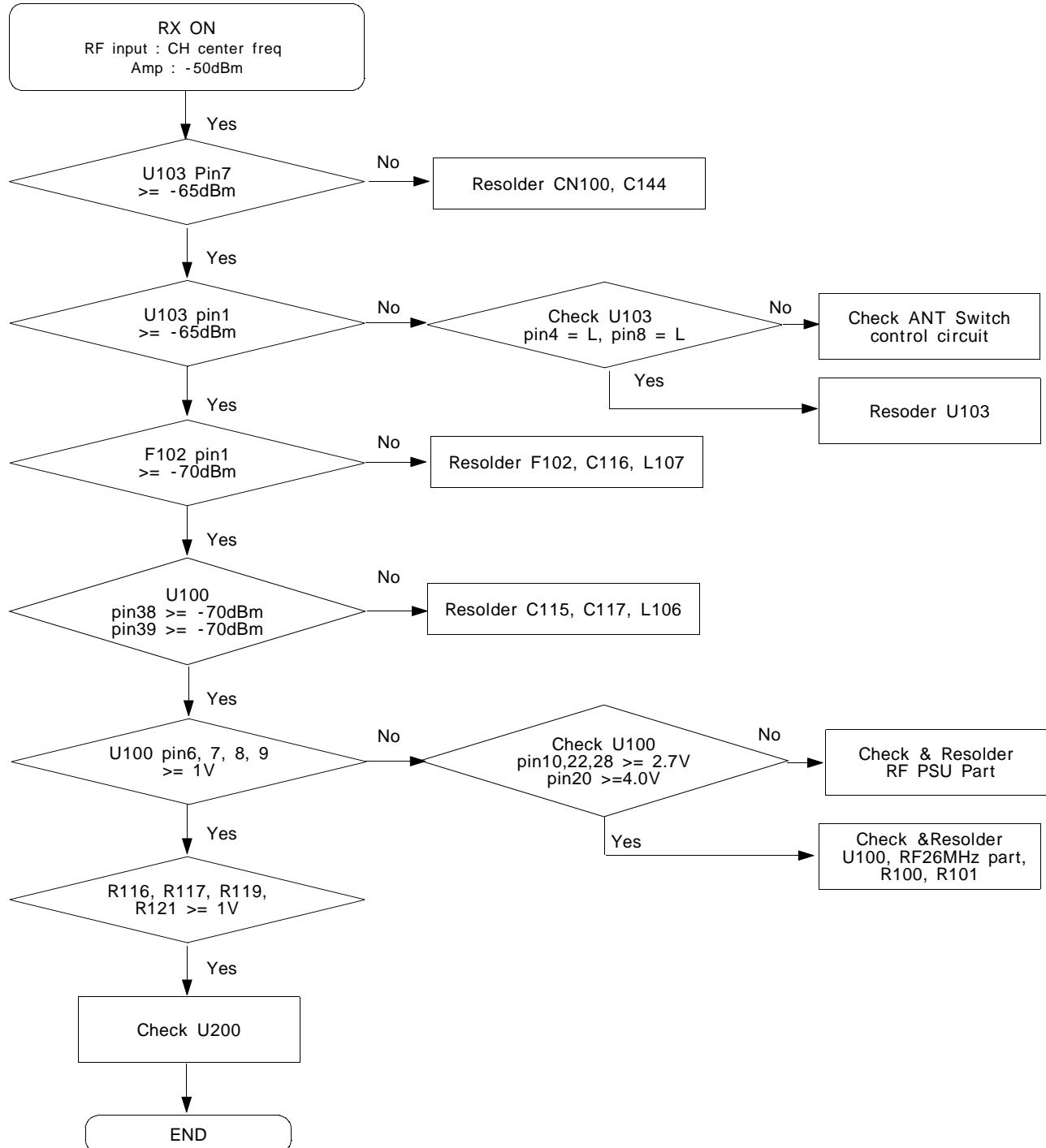
12. GSM Receiver



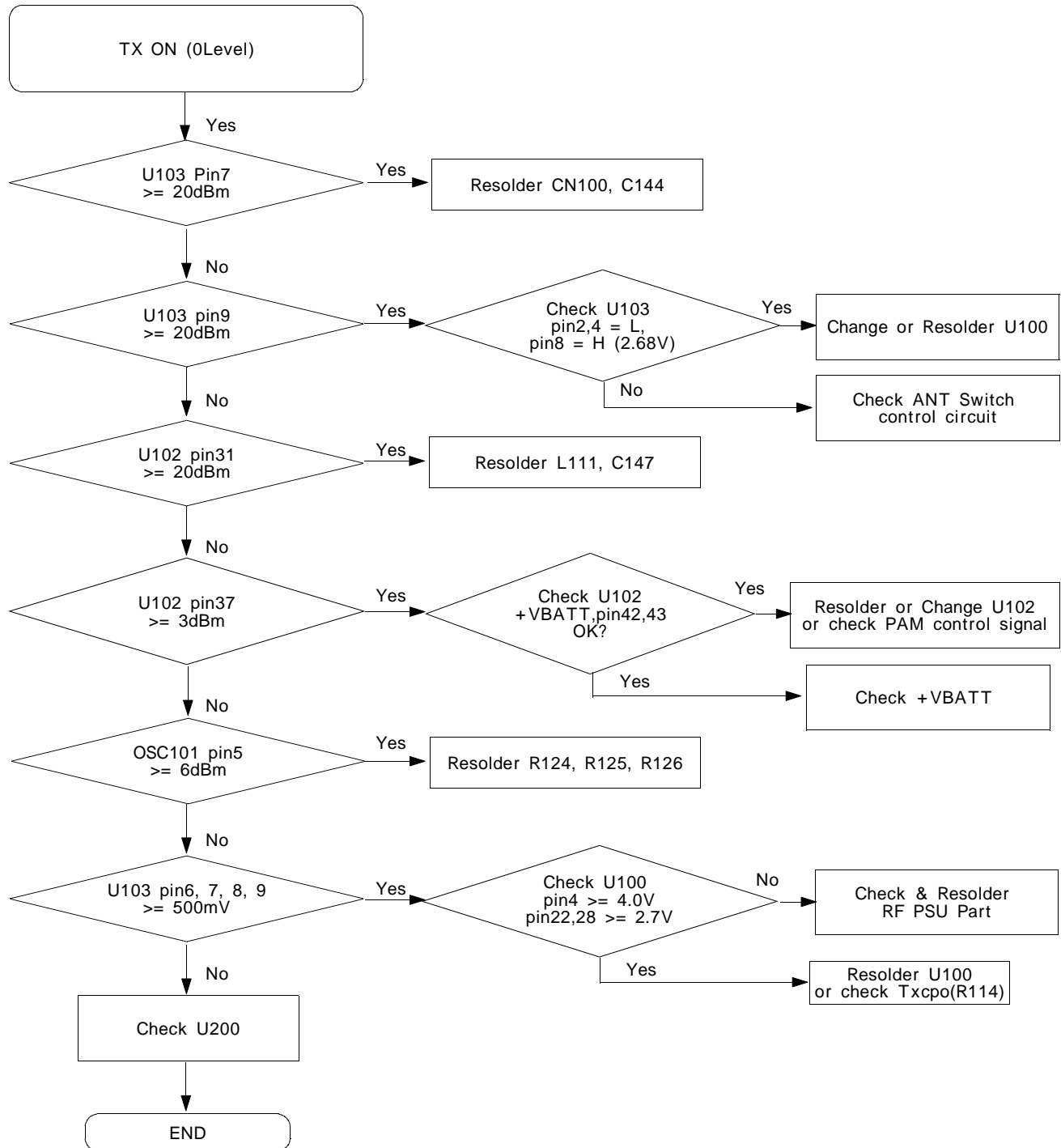
13. GSM Transmitter



14. DCS Receiver



15. DCS Transmitter



Transmitter

